University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2009) Exam 3

Name: Solution Date: Nov. 18, 2009

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) Fill in the blank:

(a) In standard CMOS process, the source and drain are formed by using p^+ and n^+ layer masks.

(b) The process of manufacturing transistors is called front-end and the process of manufacturing interconnects is called back-end.

(c) CMP stands for Chemical Mechanical Polishing.

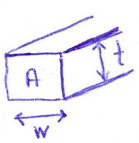
(d) The effective width of two series NMOS with W_1=6um and W_2=3um is 2μm.

(e) Electromigration is when metal lattice atoms swept out of position by current density

2. (20 points) You are asked to layout the power and ground bus in the layout of a logic block in a real chip. Assume that the logic block draws 80mA of current and the metal thickness is 0.4 um. If the maximum current density $J_{max} = 2\times10^6$ A/cm^2, determine the minimum width (in micron) of the interconnect that is needed to power the logic block.

$J_{max} \times$ Area = Current

Area = width × thickness



$$J_{max} = 2\times10^6 \text{ A/cm}^2 \times \left(\frac{100\text{ cm}}{1\text{ m}}\right)^2 \times \left(\frac{1\text{ m}}{1\times10^6\,\mu\text{m}}\right) = 0.02 \text{ A/}\mu\text{m}^2$$

$$0.02 \text{ A/}\mu\text{m}^2 = \frac{80\times10^{-3}\text{ A}}{W \times 0.4\,\mu\text{m}} \Rightarrow W = 10\,\mu\text{m}$$

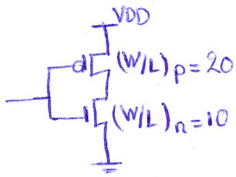
3. (30 points) A three-input CMOS NAND gate is designed as shown below. Assume that V_{DD}=1.2 V, K'_n=90 uA/V^2, V_{tn}=0.4 V, K'_p=50 uA/V^2, and V_{tp}=-0.5 V in the 100nm technology node.

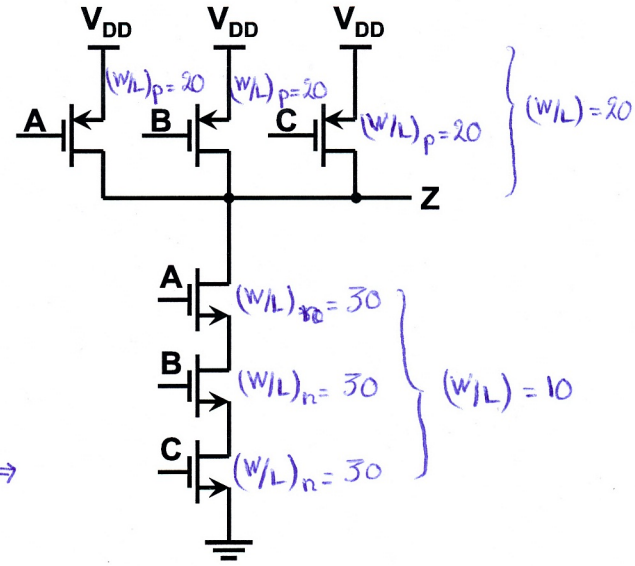
(a) Determine the width of NMOS and PMOS transistors in this NAND gate, such that the worst case delay becomes equivalent to a referenced inverter with W_n=1um and W_p=2um.

(b) For the device sizes found in part (a), determine the switching threshold voltage, V_M, when all inputs are tied together.

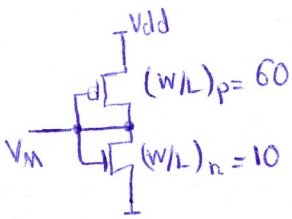
(c) Find the maximum I_{DD} current for this NAND gate.

a)





b)



$$I_p = I_n$$

$$\frac{K'_p}{2}(W/L)_p[V_{gsp}-V_{tp}]^2 = \frac{K'_n}{2}(W/L)_n[V_{gsn}-V_{tn}]^2 \Rightarrow$$

$$\frac{50\,\mu A/V^2}{2} \times 60 \times [(V_M-1.2)-(-0.5)]^2 = \frac{90\,\mu A/V^2}{2} \times 10 \times [V_M-0.4]^2 \Rightarrow$$

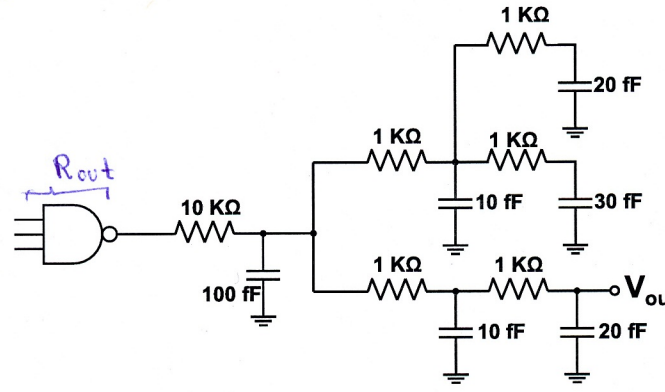
$$V_M = 0.594\ V$$

c) $$I_{DDmax} = I_n(V_m) = \frac{90\,\mu A/V^2}{2}(10)[0.594-0.4]^2 \Rightarrow I_{DDmax} = 1.69\times10^{-5}\ A$$

4. (40 points) We would like to design the following circuit such that the worst case propagation delays (t_{pHL} and t_{pLH}) are limited to 2.14 ns. Use Elmore delay equation to determine the W/L for PMOS and NMOS used in the 3-input NAND gate. Assume that V_{DD}=1.2 V, K'_n=90 uA/V^2, V_{tn}=0.4 V, K'_p=50 uA/V^2, and V_{tp}=-0.5 V in the 100nm technology node. Also assume that the transistors stay in saturation region for the length of the transition.

$t_{pLH} = 0.69\,\tau$ where $\tau = \sum_i R_i C_i$

$\tau = \frac{t_{pLH}}{0.69}$



$\tau = (R+10k) \times 100pF +$

$(R+10k) \times (10pF + 20pF + 30pF) +$

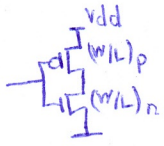
$(R+10k+1k) \times (10fF) +$

$(R+10k+1k+1k) \times (20fF)$

$\tau = \frac{2.14}{0.69} \rightarrow R_{out} = 6.06\ k\Omega$

$t_{pHL} = 0.69\,(R_{out})\,C_L \rightarrow C_L = 0.512pF$

I_{avg} ? $t_{pLH} = \frac{C_L \times (Vdd/2)}{I_{avg}} \rightarrow I_{avg} = 143.5\,\mu A$



$I_{avg} = \frac{K'_n}{2}(W/L)_n (Vdd - V_{tn})^2 \rightarrow (W/L)_n = \frac{I_{avg}}{\frac{K'_n}{2}(Vdd - V_{tn})^2} = 4.98 \simeq 5$

$(W/L)_p = \frac{I_{avg}}{\frac{K'_p}{2}(Vdd - |V_{tp}|)^2} \rightarrow (W/L)_p = 11.7 \simeq 12 \Rightarrow$