University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2009) Exam 4

Name: _____ Date: Dec. 9, 2009

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) Fill in the blank:

(a) In a flip-flop, the time that the input data needs to be stable after the rising edge of the clock is called _____.

(b) Contamination delay is _____.

(c) An 8-input dynamic logic NAND gate requires _____ transistors.

(d) NMOS is good in passing _____ and PMOS is good in passing _____.

(e) If the average propagation delay of an inverter is 100ps, then a ring oscillator of 21 stages of inverter will oscillate at the frequency of _____ MHz.

2. (20 points) Dynamic logic design problem:

(a) Draw the circuit diagram of a dynamic logic that performs $\boldsymbol{Z = \overline{A + B(C + D)}}$.

(b) Determine the width of NMOS transistors, such that the worst case t_{pHL} delay becomes roughly equivalent to a referenced inverter with Wn=1um and Wp=2um.

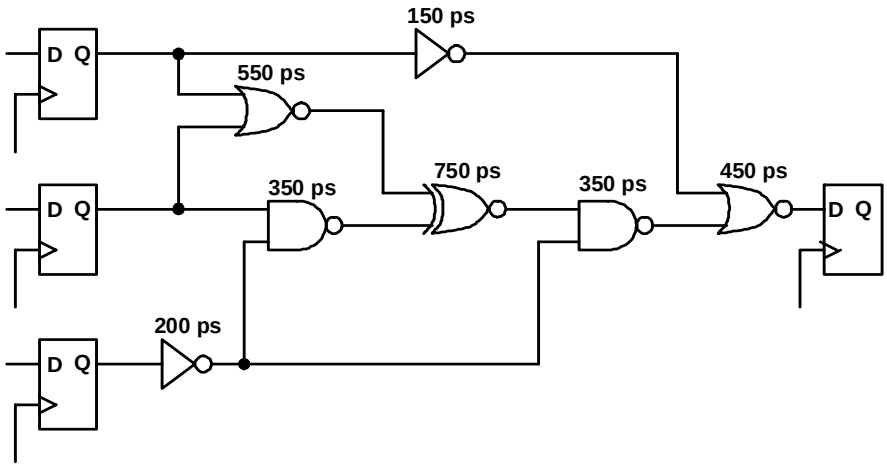
3. (30 points) Consider the following sequential circuit with 4 edge-triggered flip-flops and some logic gates. Assume that t_{SU} = 3 ns, t_{hold}= 2 ns, and t_{C2Q} = 1 ns.

(a) Identify the path with the maximum delay (critical path) on the schematic.

(b) What is the maximum operating frequency of this circuit?

(c) Identify the path with minimum delay on the schematic.

(d) Does this circuit violate the hold time constraint? Why?



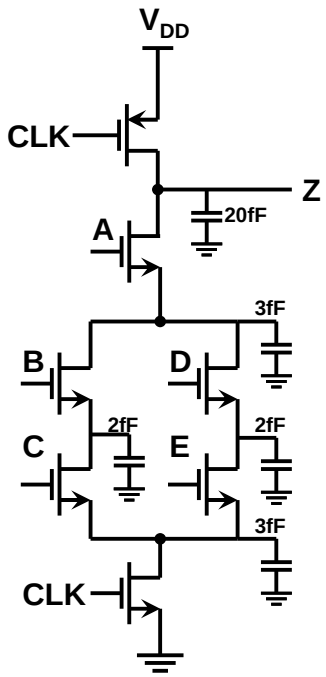
4. (40 points) The following circuit is a 4-input dynamic logic.

(a) Identify the logic function for the output Z.

(b) What input vector imposes the worst case charge sharing during the evaluation time?

(c) Compute the final voltage at Z, if the input vector is ABCDE=11000 during evaluation after charge sharing. Assume that V_{tn} = 0.4V.

(d) Determine the width of the PMOS such that the maximum worst case pre-charge time delay (0 to 90%) is limited to 250ps. (The worst case is when all the inputs are at V_{DD} such that all the intermediate capacitors contribute to the delay). Assume that V_{DD} = 1.2 V, K'_p = 50 uA/V^2, and V_{tp} = -0.5 V in the 100nm technology node. For simplicity assume that the PMOS will stay in saturation during the transition.



5. (10 bonus points) The following are bonus questions:

(a) In problem 3, how do you modify the circuit to avoid the hold time violation without any penalty on the operating frequency? (5 bonus credit)

(b) Leakage current is another problem for dynamic logics. If I_{off} is 100pA for each NMOS in problem 4, which input vectors give the maximum leakage? How much is the maximum leakage? (5 bonus credit)