

*Due in class: Wednesday October 28, 2015*

1. The circuit in Figure 1 is an NMOS switch circuit. Assume  $V_{DD}=5V$ ,  $\gamma=0.4V^{1/2}$ ,  $2|\phi_f|=0.6V$ ,  $V_{T0}=1V$ ,  $k_n'=100\mu A/V^2$ ,  $(W/L)=10$ , and  $\lambda=0.1V^{-1}$ . The channel length modulation is applicable only in the saturation region.
  - a. Determine the charging current to  $C_L$  right after the rising edge of the input. Assume that the capacitor is completely discharge at the beginning of the transition. Make sure that you include all applicable device parameters in your calculations.
  - b. Determine the charging current to  $C_L$  when the output voltage is at 50% of  $V_{DD}$ . Again, make sure that you include all applicable device parameters in your calculation.
  - c. Use the results from parts a and b to estimate the low-to-high propagation delay ( $t_{pLH}$ ) of the NMOS switch in Figure 1.
  - d. Use PSPICE and measure the  $t_{pLH}$  of the circuit in Figure 1 and compare your results with part c. (Hint: the .model for this device is shown below of this page)

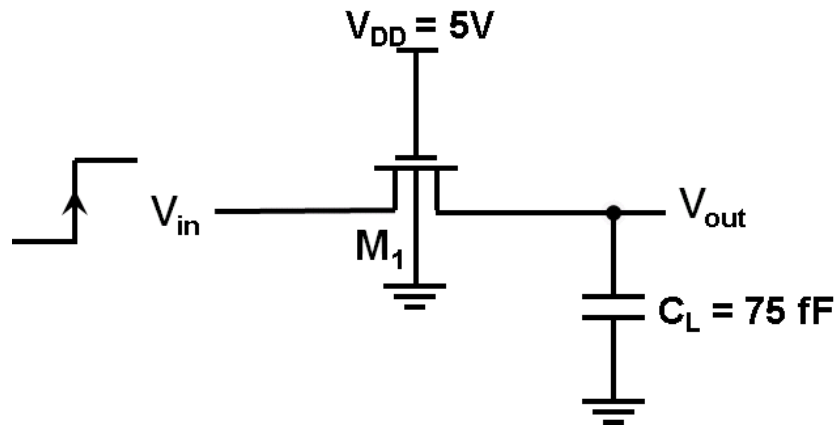


Figure 1 – NMOS Switch Circuit

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.model NCH NMOS LEVEL=1 VTO=1 KP=100U GAMMA=0.4 LAMBDA=0.1 PHI=0.3
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