University of New Mexico

Department of Electrical and Computer Engineering

ECE 321L – Electronics I (Fall 2015) Homework #6

Due in class: Wednesday September 30, 2015

1. The doping concentrations of a PN junction diode are $N_A=5.12\times10^{16}$ atoms/cm^3 and $N_D=1.47\times10^{18}$ atoms/cm^3. Assume that the cross section area of the diode is 1mm^2. Determine the following parameters for the diode at room temperature:

a. Built in potential (V_γ).

b. Depletion width (W_{do}) in um at zero bias.

c. Junction capacitance (C_j) in pF at zero bias.

d. Depletion width (W_d) in um at -5V bias.

e. Junction capacitance (C_j) in pF at -5V bias.

f. The breakdown voltage for the diode, if the breakdown electric field for silicon is $\xi_c=3\times10^5$ V/cm.

g. Depletion width (W_d) in um at the breakdown voltage estimated in f.

2. We would like to design and fabricate a diode that is going to be used in a high voltage power source. The diode has to withstand 220V reverse bias, therefore we have decided to set the breakdown voltage to 250V. Assuming that we can make the doping concentration for N and P the same ($N_A=N_D$) and the breakdown electric field for silicon is $\xi_c=3\times10^5$ V/cm, determine:

a. The doping concentrations for N and P.

b. Built in potential (V_γ).

c. Depletion width (W_d) in um at zero bias.

d. Depletion width (W_d) in um at the breakdown voltage (V_D=-250V).

3. As discussed in the class there are parasitic capacitances almost between each two terminal of a transistors. In this homework, we would like to estimate all parasitic capacitances in an NMOS that is fabricated using an old 0.5um process from an undisclosed foundry. The device parameters for this problem are: x_d=110nm, L_S=L_D=1.5um, L=0.5um, W=5um, t_{ox}=5.7nm, ε_{ox}=3.9ε_o, C_j=1.79 fF/um^2, φ_o=0.99V, m_j=0.468, C_{jsw}=0.376 fF/um, φ_{osw}=0.97V, m_{jsw}=0.299. (fF is femto-Farad, which is 10^{-15} F)

a. Determine L_{eff}.

b. Determine C_{ox}, the gate oxide capacitance per unit area (fF/um^2).

c. Estimate the overlap capacitances, C_{GSOV} and C_{GDOV}.

d. Estimate the channel capacitances, C_{GBCH}, C_{GSCH}, and C_{GDCH}, for three regions of operations (cut-off, linear, and saturation).

e. Estimate the junction capacitances C_{JDB} and C_{JSB}. Assume V_{SB}=0 and V_{DB}=5V.

f. Estimate all the parasitic capacitances (C_{GD}, C_{GS}, C_{GB}, C_{DB}, and C_{SB}) for cut-off, linear, and saturation regions and fill the table below with the values in fF.

	C_{GD}	C_{GS}	C_{GB}	C_{DB}	C_{SB}
Cut off					
Linear					
Saturation					

Hint: Helpful Equations:

$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}$$

$$C_{BS}(V_{BS}) = \frac{CJ \cdot AS}{(1 - V_{BS}/PB)^{MJ}} + \frac{CJSW \cdot PS}{(1 - V_{BS}/PB)^{MJSW}}$$