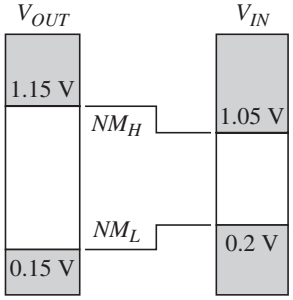
References

[1] F. A. Linholm IEEE J. Solid State Circuits, SC-10, 2, pp. 106–109, April 1975.

Exercises

Inverter Static Voltage Characteristics

5-1. A CMOS inverter has $V_{DD} = 1.2$ V. $V_{OH} = 1.15$ V, $V_{OL} = 0.15$ V, $V_{IH} = 1.05$ V, and $V_{IL} = 0.2$ V. Calculate NM_H, NM_L and draw the noise margin map with appropriate labels of numbers.



5-2. A logic gate noise margin parameters are: $V_{IH} = 1.6$ V, $V_{IL} = 0.3$ V, $V_{OH} = 1.7$ V, and $V_{OL} = 0.2$ V.

(a) Calculate NM_H.

(b) Calculate NM_L.

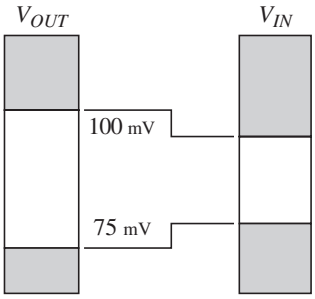
(c) The input voltage is down to 1.7 V and a negative 50 mV noise spike appears. What happens to the circuit fidelity?

(d) The input voltage is down to 1.7 V and a negative 150 mV noise spike appears. What happens to the circuit fidelity?

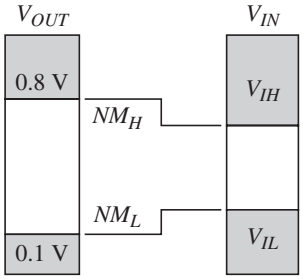
5-3. Given the logic gate noise margins: $NM_H = 100$ mV, $NM_L = 75$ mV, and $V_{DD} = 2$ V.

(a) If $V_{IH} = 1.75$ V, what is V_{OH}?

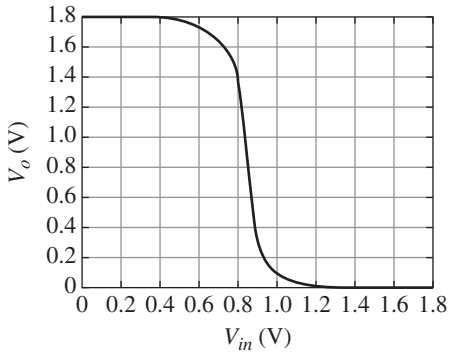
(b) If $V_{IL} = 0.3$ V, what is V_{OL}?



5-4. A CMOS inverter uses $V_{DD} = 0.9$ V. $V_{OH} = 0.8$ V, and $V_{OL} = 0.1$ V. If the noise margins must be 20% of V_{DD}, what are V_{IL} and V_{IH}? Draw the noise margin map and label.

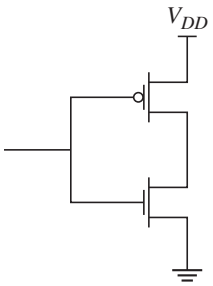


5-5. Graphically determine the change in logic threshold of the CMOS inverter transfer curve in the figure if the curve shifts 0.2 V to the right in the midregion.



5-6. **(a)** Design the W_p/W_n ratios of a CMOS inverter for symmetrical static voltage transfer characteristic. $\mu_n = 1400$ cm^2/V · s, $\mu_p = 500$ cm^2/V · s, $V_{tn} = 0.35$ V, $V_{tp} = -0.35$ V, and $V_{DD} = 1.3$ V.

(b) Redesign if $V_{tp} = -0.45$ V.



5-7. An inverter with a symmetrical voltage transfer curve has a restriction that $W_p/W_n = 4.6$. $V_{DD} = 1.2$ V, $\mu_n = 1530\ \text{cm}^2/\text{V} \cdot \text{s}$, $\mu_p = 540\ \text{cm}^2/\text{V} \cdot \text{s}$, and $V_{tp} = -0.4$. What must V_{tn} be set to satisfy this condition?

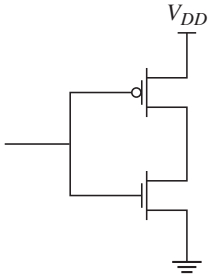
5-8. A CMOS inverter has transistor parameters: $K_n(W/L)_n = 100\ \mu\text{A/V}^2$, $K_p(W/L)_p = 300\ \mu\text{A/V}^2$, $V_{tn} = 0.7$ V, $V_{tp} = -0.75$ V, and $V_{DD} = 2.5$ V. What fraction of the total output voltage swing will the *n*MOS transistor be in saturation?

5-9. A CMOS inverter has its *n*MOS transistor in nonsaturation and its *p*MOS transistor in saturation. Given $K_n = 50\ \mu\text{A/V}^2$, $K_p = 25\ \mu\text{A/V}^2$, $V_{tn} = 0.5$ V, $V_{tp} = -0.6$ V, $(W/L)_n = 2$, $(W/L)_p = 4$, $I_{DD} = 11\ \mu$A, and $V_{DD} = 2$ V, calculate the inverter output voltage V_O.

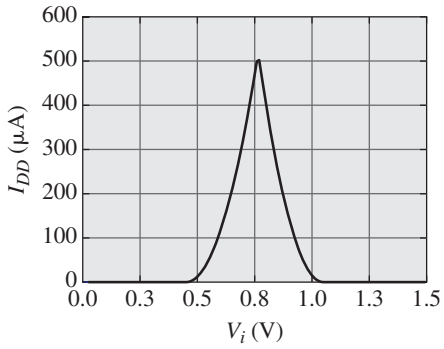
Inverter Static Current Characteristics

5-10. Given an inverter with $V_{DD} = 1.5$ V, $V_{tn} = 0.4$ V, and $V_{tp} = -0.4$ V, calculate the peak current during the transition if $(W/L)_n = 3$, $(W/L)_p = 7.5$, $K_p = 50\ \mu\text{A/V}^2$, and $K_n = 125\ \mu\text{A/V}^2$.

5-11. An inverter has $V_{DD} = 2$ V, $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $K_n = 300\ \mu\text{A/V}^2$, $K_p = 200\ \mu\text{A/V}^2$, $(W/L)_n = 2$, and $(W/L)_p = 3$.
(a) If $V_{IN} = 0.8$ V, what is I_{DD}?
(b) The I_{DD} solution in part (a) appears twice in the current transfer curve. Use the *p*MOS equations to calculate the other V_{IN} value to satisfy the current in part (a).



5-12. Given $V_{DD} = 1.5$ V, $K_p = 70\ \mu$A. $K_n = 120\ \mu$A, $(W/L)_p = 150$, and $(W/L)_n = 75$, use the ITC to calculate V_{tp}.



5-13. Given that $V_{DD} = 1.8$ V, $V_{tn} = 0.5$ V, and $K_n = 100\ \mu\text{A/V}^2$, what is W/L of the *n*MOS transistor?