ECE321 – Electronics I

Lecture 14: CMOS Inverter: Short Circuit Power

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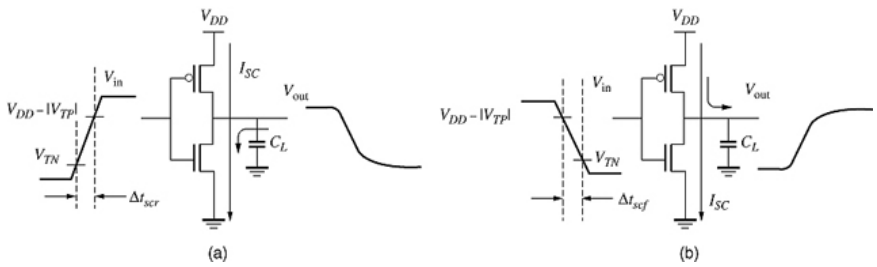
Review of Last Lecture

- **Mostly Review of Lecture 2 for Dynamic Power Calculation**

Today's Lecture

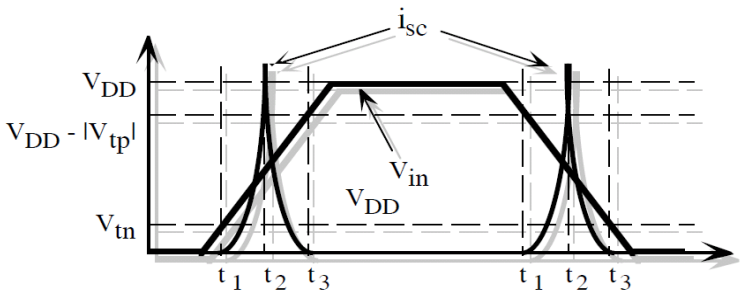
- Short Circuit Power Analysis
- Short Circuit Power Reduction Techniques

CMOS Short Circuit Power Consumption



- Short circuit or crowbar current is the current that flows directly from VDD to GND during switching transition, when both transistors are ON, i.e. $V_{tn}<V_{in}<V_{DD}-V_{tp}$
- Short circuit current can be significantly large when NMOS and PMOS are large. (Why?)

Computing Short-Circuit Power



- For clock circuit that toggles twice in each period (low-to-high and high-to-low), the active power consumption is computed as:

Computing Short-Circuit Power

- Assuming a symmetric inverter, where $V_{tn}=|V_{tp}|$ and $K'_n(W/L)_n=K'_p(W/L)_p$, then the short circuit currents for rise and fall will be symmetric, and therefore

$$I_{mean} = \frac{1}{T}\int_0^T I(t)dt = \frac{4}{T}\int_{t_1}^{t_2} \frac{K'_n}{2}\frac{W}{L}\left(V_{in}(t) - V_t\right)^2 dt$$

$$V_{in} = \frac{V_{DD}}{\tau}t \qquad t_1 = \frac{V_t}{V_{DD}}\tau \quad \text{and} \quad t_2 = \frac{\tau}{2}$$

$$I_{mean} = \frac{K'_n}{12}\left(\frac{W}{L}\right)\frac{1}{V_{DD}}\left(V_{DD} - 2V_t\right)^3\frac{\tau}{T} \quad \Rightarrow \quad P_{sc} = V_{DD}\, I_{mean}$$

Example: Short Circuit Power in an Inverter

What is the short circuit power in an inverter if: $V_{DD} = 2$ V, $V_{tn} = -V_{tp} = 0.5$ V, $T = 500$ ps, $f = 2$ GHz, $K_n = 200\ \mu A/V^2$, $W/L = 2$, and the pulse rise and fall times are 100 ps.

$$I_{mean} = \left(\frac{1}{12}\right)\left(\frac{200\mu A}{2\,V}\right)\left(\frac{2}{1}\right)(2 - 1)^3\left(\frac{100\,ps}{500\,ps}\right) = 3.33\mu A$$

so

$$P_{sc} = 2V \times 3.33\ \mu A = 6.7\ \mu W$$

Minimum SC Power Design Techniques

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9 V by 2015!)
- Faster rise and fall times
- Smaller transistors (will increase delay)
- Higher V_t (will increase delay)
- Lower frequency (will decrease performance)

$$I_{mean} = \frac{K'_n}{12}\left(\frac{W}{L}\right)\frac{1}{V_{DD}}\left(V_{DD} - 2V_t\right)^3\frac{\tau}{T}$$