

ECE321 – Electronics I

Lecture 15: CMOS Inverter: Leakage Power

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Tuesday 2:00-3:00PM or by appointment
E-mail: payman@ece.unm.edu

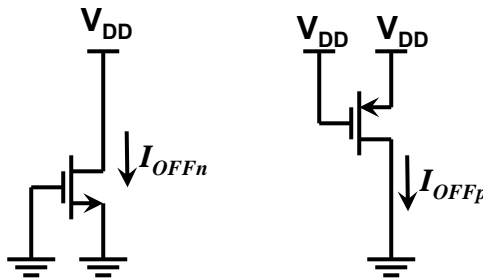
Review of Last Lecture

- Short Circuit Power Analysis
- Short Circuit Power Reduction Techniques

Today's Lecture

- Leakage Current and Power

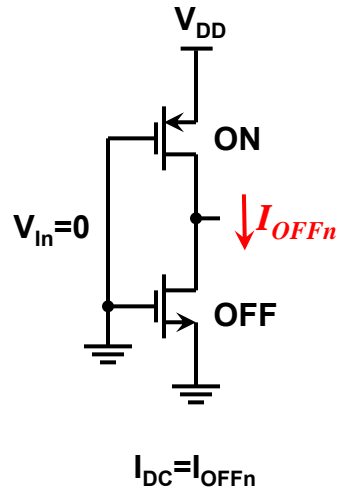
Leakage in MOSFETs



- MOSFET consists of two diodes connected back to back, one in forward and the other one in reverse bias.
- When the transistor is off, $V_{GS} < V_T$, the reverse biased diode will draw current, which is called “leakage current” or “off current”.
- I_{OFF} is heavily dependent on threshold voltage. Higher threshold voltage results in lower leakage, but lower performance too.

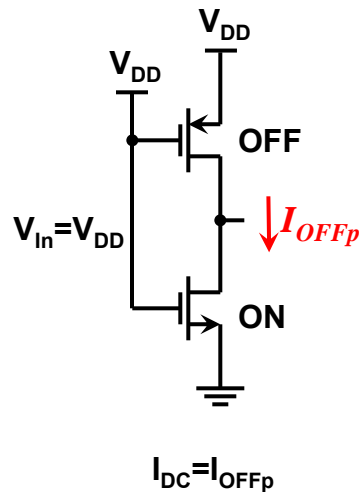
Leakage in CMOS Inverter ($V_{in}=0$)

- ❑ When the input of a CMOS inverter is at 0, PMOS is ON and can deliver any current.
- ❑ NMOS is OFF and will draw I_{OFFn} leakage from the power supply.
- ❑ The leakage power consumption in this case is equal to $I_{DC} \cdot V_{DD}$



Leakage in CMOS Inverter ($V_{in}=V_{DD}$)

- ❑ When the input of a CMOS inverter is at V_{DD} , NMOS is ON and can deliver any current.
- ❑ PMOS is OFF and will draw I_{OFFp} leakage from the power supply.
- ❑ The leakage power consumption in this case is equal to $I_{DC} \cdot V_{DD}$



Leakage Power in CMOS Inverter

- ❑ The amount of leakage power in a CMOS inverter is input dependent.
- ❑ Assuming that the probability of input being 0 and VDD is 50% each, then the average leakage power will be:

$$P_{\text{leak}} = I_{\text{DC,av}} \cdot V_{\text{DD}} = (0.5 \cdot I_{\text{OFFn}} + 0.5 \cdot I_{\text{OFFp}}) \cdot V_{\text{DD}}$$

- ❑ Sometimes, IOFF of a MOS transistor is normalized to the width of the transistor, W. In this case you need to multiply it by the width to get the actual current.

Example: Leakage Power in an Inverter

- ❑ Compute the average leakage power in a CMOS inverter, where $(W/L)_n=10$, $(W/L)_p=15$, $I_{\text{OFFn}}=27\text{nA}/\mu\text{m}$, and $I_{\text{OFFp}}=32\text{nA}/\mu\text{m}$. The inverter uses 1.2V supply voltage and is implemented in 65nm technology node.

$$P_{\text{leak}} = I_{\text{DC,av}} \cdot V_{\text{DD}} = (0.5 \cdot I_{\text{OFFn}} + 0.5 \cdot I_{\text{OFFp}}) \cdot V_{\text{DD}}$$

$$P_{\text{leak}} = (0.5 \cdot 27 \times 10^{-9} \cdot (10 \cdot 65 \times 10^{-3}) + 0.5 \cdot 32 \times 10^{-9} \cdot (15 \cdot 65 \times 10^{-3})) \cdot 1.2$$

$$P_{\text{leak}} = 29.25 \text{ nW}$$

- ❑ If we have a design with effectively 200 million inverter, how much the total leakage power will be.

$$P_{\text{leak,tot}} \approx 6 \text{ W}$$

Minimum Leakage Power Design Techniques

- Prime choice: Threshold Voltage increase, or I_{OFF} reduction
 - This will impact the performance too (Check delay equation)
- Power supply reduction
- Smaller transistors (will increase delay)
- Higher V_t (will increase delay)