ECE321 – Electronics I

Lecture 19: CMOS Fabrication

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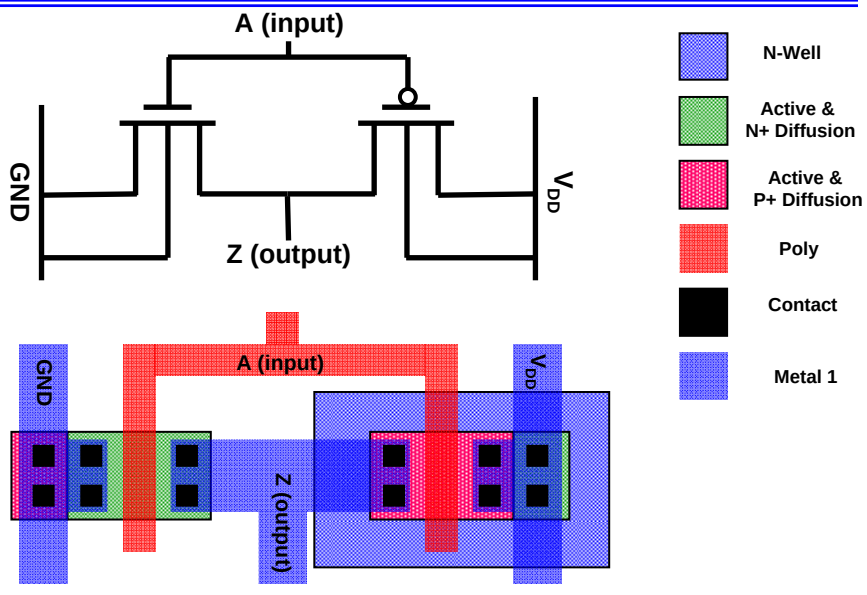
Review of Last Lecture

- **Miller Effect**
- **Interconnect Delay**
- **Elmore Delay**

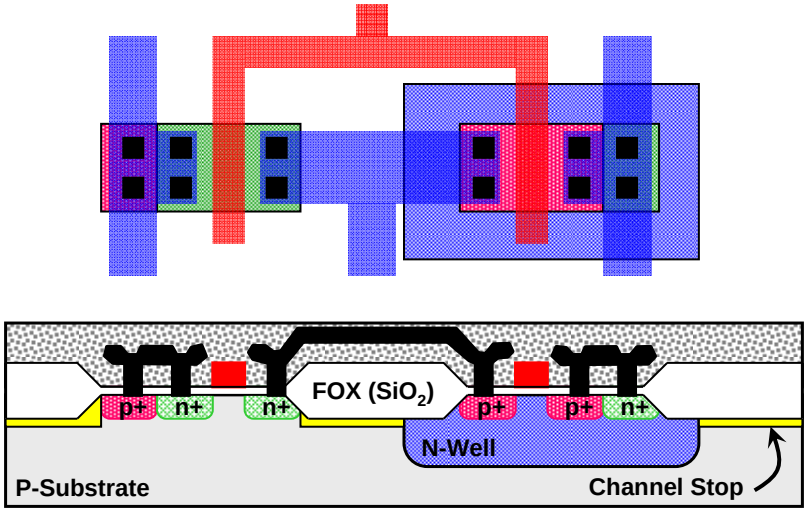
Today's Lecture

- CMOS Manufacturing Process
  - Front-end Process
  - Back-end Process
- Interconnect Manufacturing Process
  - Back-end Process (Conventional)
  - Back-end Process (Modern – Dual Damascene)

Inverter Schematic & Layout

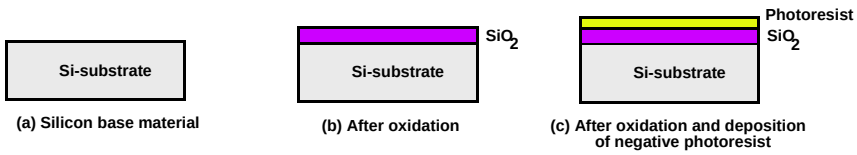


Cross Section of CMOS Inverter

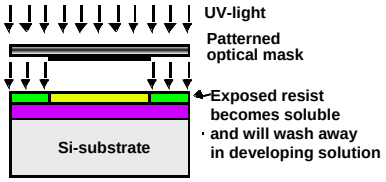


Overview of Lithography

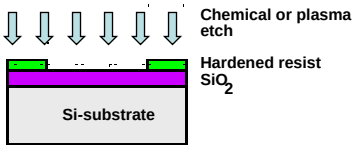
- In order to etch a window opening in a SiO_2 layer on a Si substrate the first step is to spin on a photoresist
- Photoresist is a light sensitive and acid resistant polymer
  - Positive photoresist is initially insoluble to developing agent and becomes soluble when exposed to UV light
  - Negative photoresist is initially soluble and becomes resistant to the developing agent when exposed to UV light



Lithography Process

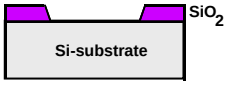


(d) Stepper exposure



(e) After development and etching of resist, chemical or plasma etch of SiO_2

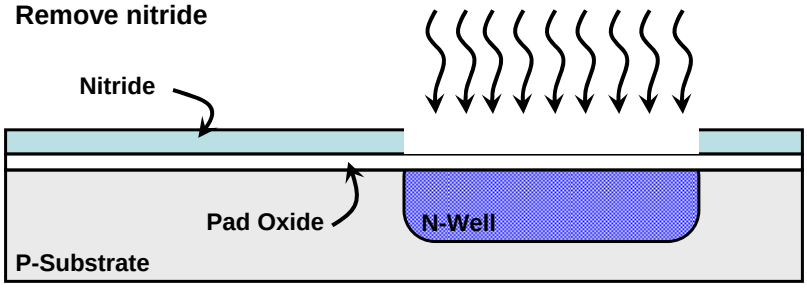
(f) After etching



(g) Final result after removal of resist

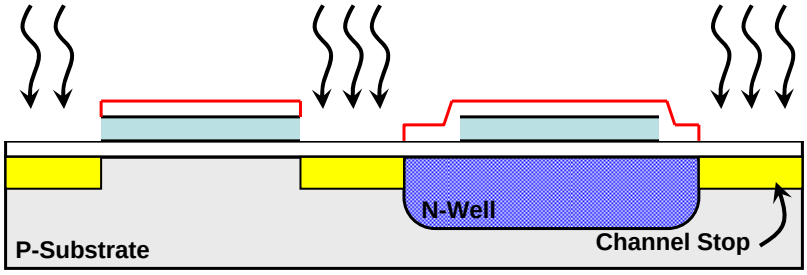
CMOS Process (N-Well)

1. Start with p-doped substrate
2. Deposit pad ox (stress relief) and Si_3N_4 (implant block)
3. Pattern nitride (Si_3N_4)
4. Implant N-type impurities (phosphorous) with high energy, low doping
5. Remove nitride



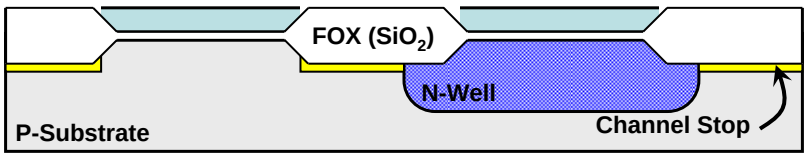
CMOS Process (Channel Stop)

6. Deposit new pax ox/nitride and pattern using active where "active = (n+ mask) + (p+ mask)"
7. Apply p-field resist and pattern using inverse N-well
8. Implant P-type impurities low energy (channel stop)



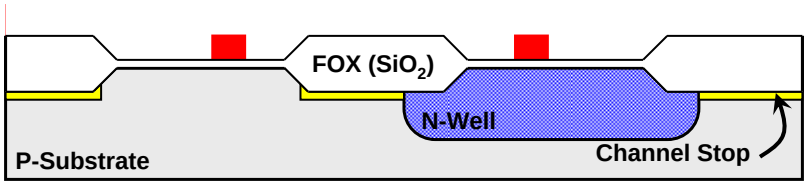
CMOS Process (FOX)

9. Grow field oxide (SiO2)
   - Nitride prevents oxidation => Local Oxidation of Silicon (LOCOS)
   - Oxidation consumes silicon => Silicon recessed
10. Remove nitride



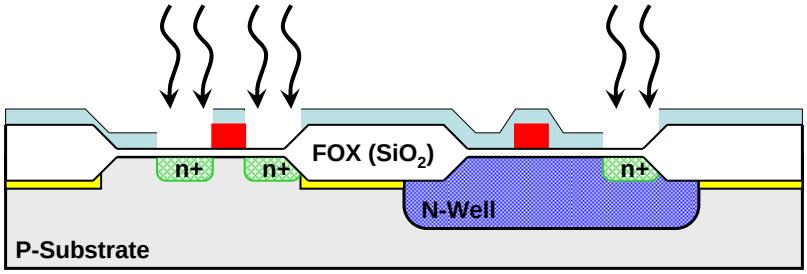
CMOS Process (Poly Gate)

11. Oxidize entire wafer (this forms gate oxide)
12. Deposit polysilicon (CVD)
13. Dope Poly Heavily
14. Pattern polysilicon (Plasma Etch)



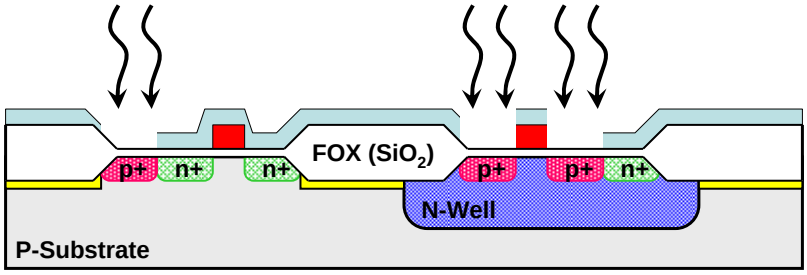
CMOS Process (n+ implants)

15. Deposit and pattern another nitride layer to expose n+ Source/Drain implant
16. Implant p+ source/drain dopants (high dose, med energy)
17. Remove nitride



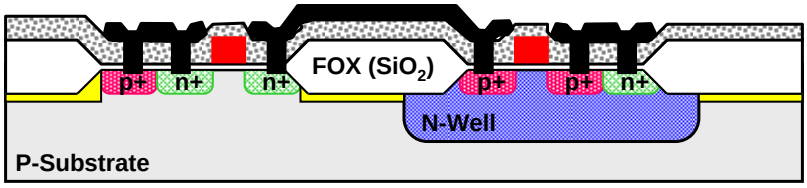
CMOS Process (p+ implants)

18. Deposit and pattern another nitride layer to expose p+ Source/Drain implant
19. Implant n+ source/drain dopants (high dose, med energy)
20. Remove nitride



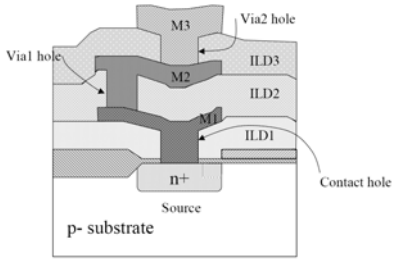
CMOS Process (Contacts & M1)

21. Deposit ILD (SiO_2)
22. Pattern and etch contact holes
23. Sputter on M1
24. Pattern and etch M1



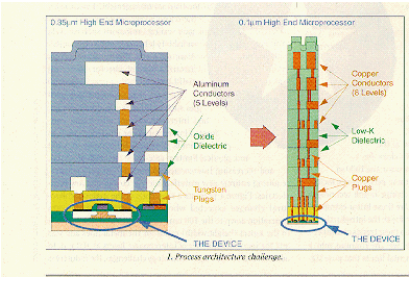
Problem with Conventional Process

- Adding more metal layers increases unevenness of the surface.
- Uneven surface (topography) causes yield problem with metal mask.
- Because of uneven surface, conventional interconnect process (reflow) requires several restriction on the layout design.
  - Stacking via is prohibited in conventional process.
  - The maximum number of metal layers is limited to 3.



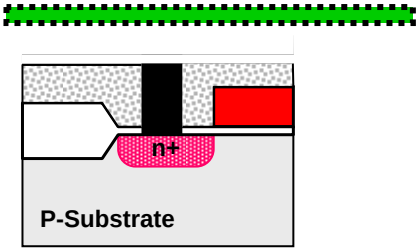
Problem with Conventional Process

- Advanced VLSI technology requires many layers of interconnects
  - As transistor density/quantity increases there is more and more need for interconnect
- Planarization is therefore needed for back-end process in advanced VLSI technology.



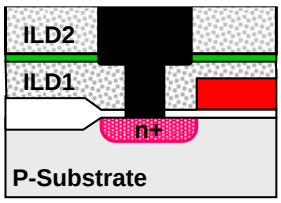
Planarization Process (Contact)

1. Thick ILD (SiO_2) is laid down
2. Wafer's face is Chemically Mechanically Polished (CMP) in a slurry of etchents and aggregates
3. Contact holes are etched
4. Tungsten is sputtered on (forms tungsten plugs)
5. CMP is applied again (this time in a slurry that etches metal more so than SiO_2)



Dual Damascene Copper Metallization (M1)

1. Contact holes are filled with tungsten and plannarized.
2. An etch stop layer and ILD2 are deposited
3. The M1 pattern is etched in the ILD2
4. A barrier Cu seed layer is sputtered next
5. Copper is plated onto the surface of the wafer
6. CMP removes copper and barrier metal except in the M1 trench.



Dual Damascene Copper Metallization (M2)

1. After M1 CMP, a nitride etch stop and the ILD3 layers are deposited.
2. Next the Via1 holes are patterned and etched
3. The Via1 holes are filled with a sacrificial layer similar to photoresist (SLAM)
4. The M2 is patterned and etched into the ILD3
5. The SLAM is removed and a barrier/seed layer is deposited.
6. Copper plating and CMP finishes off the M2 process