ECE321 – Electronics I

Lecture 20: Design Rules & Basic Layout Techniques

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Review of Last Lecture

- **CMOS Manufacturing Process**
  - **Front-end Process**
  - **Back-end Process**
- **Interconnect Manufacturing Process**
  - **Back-end Process (Conventional)**
  - **Back-end Process (Modern – Dual Damascene)**

Today's Lecture

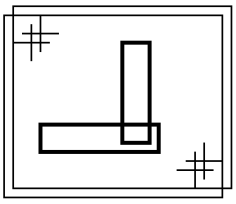
- Review of output resistance of an inverter
- Overview of Design Rules
  - What are design rules?
  - Why have design rules?
  - Typical design rules
- Layout Techniques
  - Design for density
  - Design for performance
  - Design for reliability

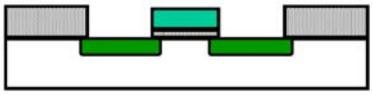
What Are Design Rules?

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum feature size (transistor gate length)
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

- To be able to tolerate some level of fabrication errors such as
  - Mask misalignment
  - Dust
  - Process parameters (e.g., lateral diffusion)
  - Rough surfaces





Typical CMOS Process Layers

Layers:

N-Well

Active Area

Select (n+,p+)

Polysilicon

Metal1

Metal2

Contact To Poly

Contact To Diffusion

Via

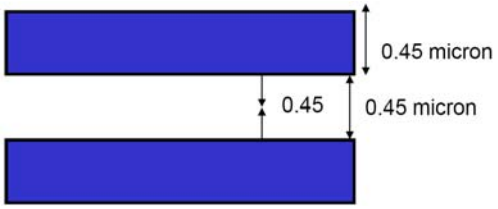
- Points:
  - N-well process p-type wafer (no p-well)
  - Active area determines where transistors may go
  - Poly overlapping with active = transistor
  - Select is where n+ and p+ ion implantation occurs; it can be used to place an opposite type region (e.g., put p+ select within n-well to create a p+ well plug, more later)
  - All contacts/vias are the same size (eases processing)
  - Advanced technology is more complex and has more layers (e.g. Thick Oxide, Thin Oxide, VT_high, VT_low, LI, etc.)

CMOS Process Layers in Layout Tools

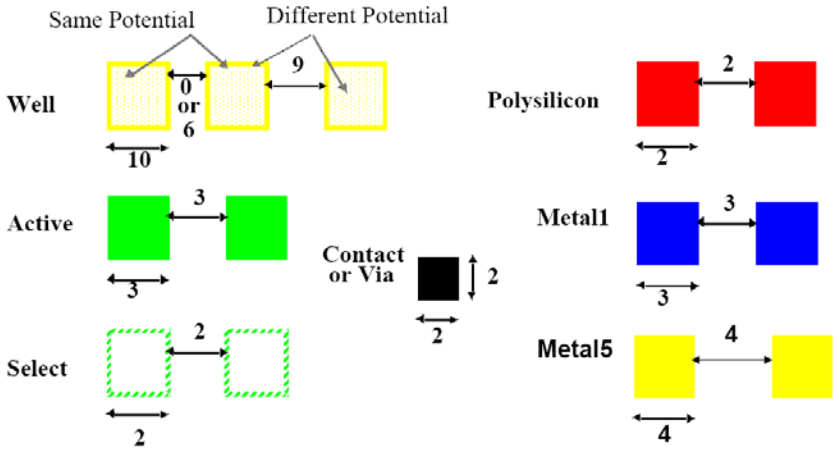
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are not related) on the same layer to ensure they will not short after fab

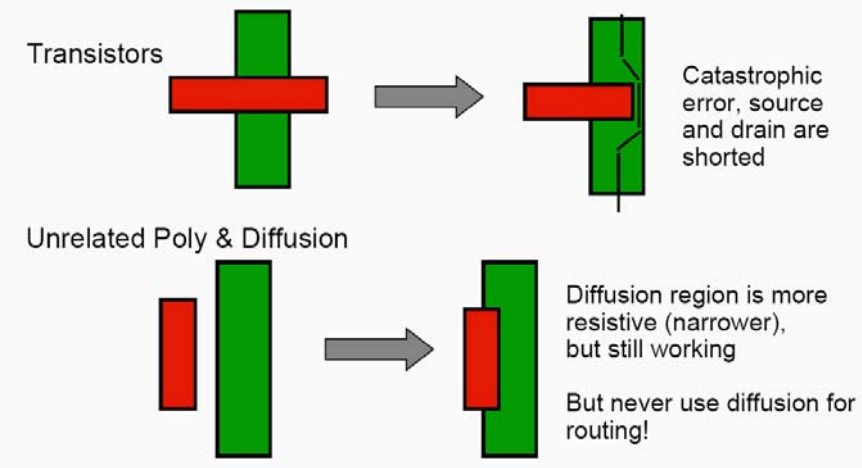


Intra-Layer Design Rules



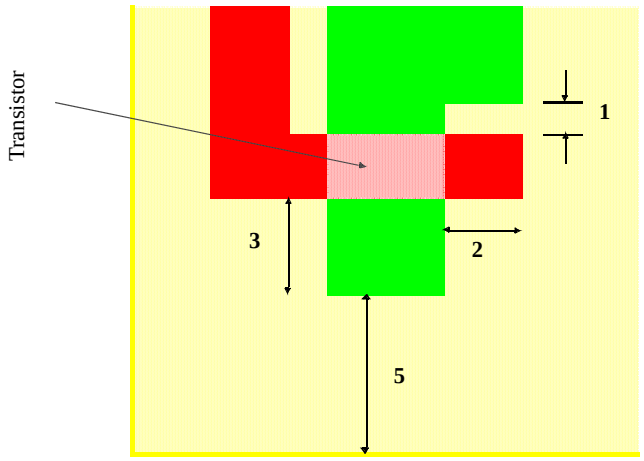
Inter-Layer Design Rule Origins

- **Transistor rules – transistor formed by overlap of diffusion (also called active) and poly layers**

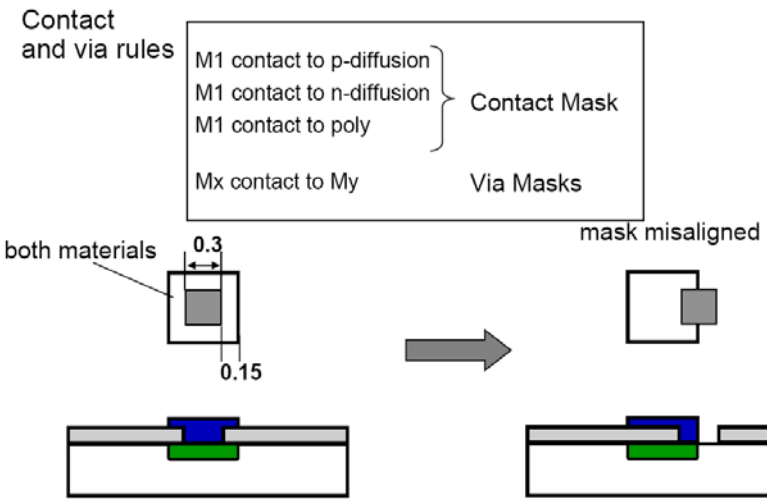


Transistor Layout

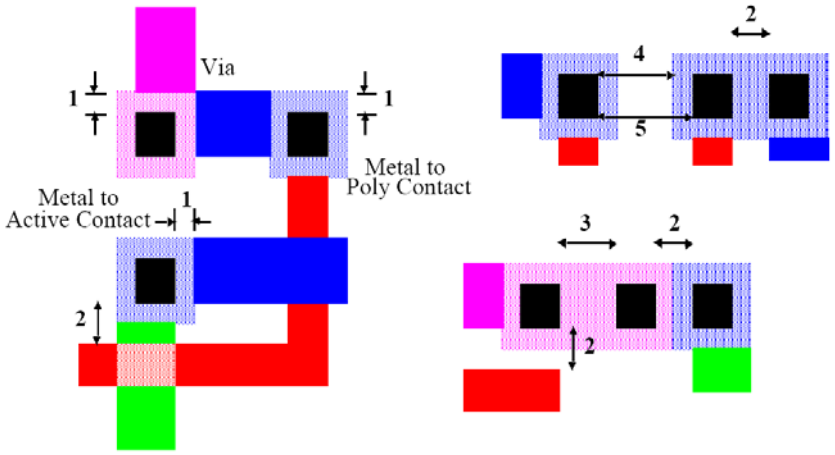
- We will almost always use minimum L device



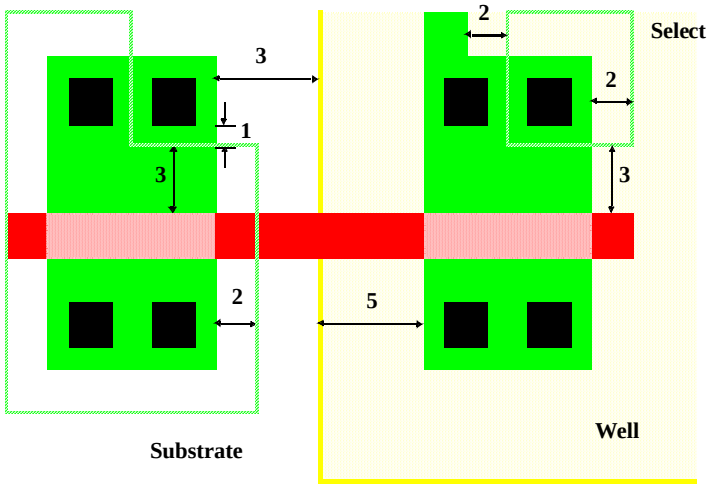
Inter-Layer Design Rule Origins



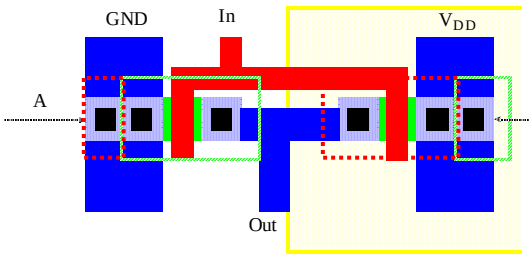
Vias and Contacts Design Rules



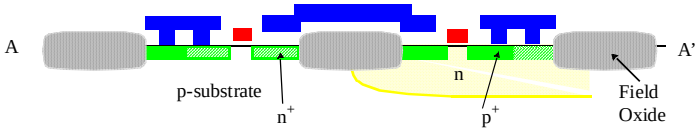
n+ or p+ Select Design Rules



Example: CMOS Inverter Layout

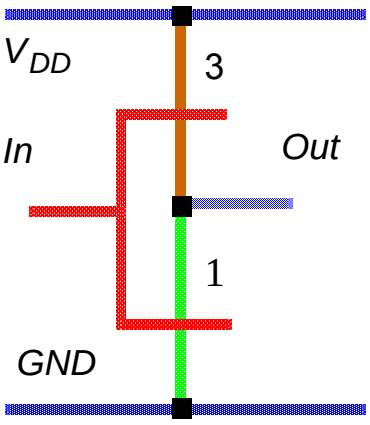


(a) Layout



(b) Cross-Section along A-A'

CMOS Inverter Layout Sticks Diagram



Stick diagram of inverter

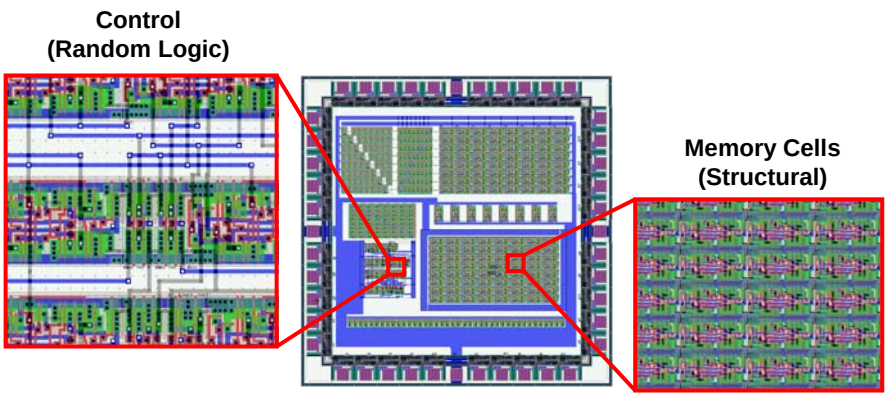
- Dimensionless layout entities
- Only topology is important

Design Rules Used for the Class Project

Table 11.1.
2 µm Design Rules (DR)

DR #	DR Description	DR
1	*n*-well enclosure of *p*-type active.....	5 µm
2	*n*-well space to *p*-type active.....	3 µm
3	*n*-well space to *n*-type active.....	5 µm
4	*n*-well width.....	5 µm
5	*n*-well space to *n*-well.....	5 µm
6	active width.....	3 µm
7	active space to same type active.....	3 µm
8	active space to opposite type active..	5 µm
9	polysilicon width.....	2 µm
10	polysilicon space to polysilicon.....	2 µm
11	polysilicon space to active.....	1 µm
12	gate space to gate.....	4 µm
13	polysilicon endcap length.....	2 µm
14	contact width.....	2 µm
15	contact width.....	2 µm
16	contact space to contact.....	4 µm
17	active enclosure of contact.....	1 µm
18	polysilicon enclosure of contact.....	2 µm
19	polysilicon contact space to active...	3 µm
20	active contact space to polysilicon...	2 µm
21	metal-1 width.....	2 µm
22	metal-1 space to metal-1.....	3 µm
23	metal-1 enclosure of contact.....	1 µm

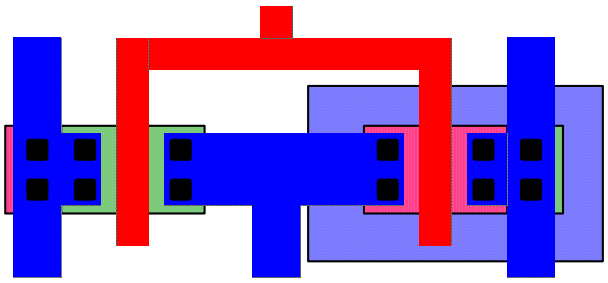
An Example of Layout



Good Layout Characteristics

- **Density**
  - Cells pack together well
  - Cells are routable—think about how they will fit together before starting!
  - Start with paper diagram first
- **Performance**
  - Keep capacitances low (specially diffusion cap)
  - Keep interconnects short
- **Reliability**
  - Poor layout can greatly affect the circuit reliability
  - Use proper wire width for power rails (IR drop, electromigration)
- **Final Checks**
  - Layout must match the circuit being built (LVS)
  - Layout must meet the manufacturing design rules (DRC)

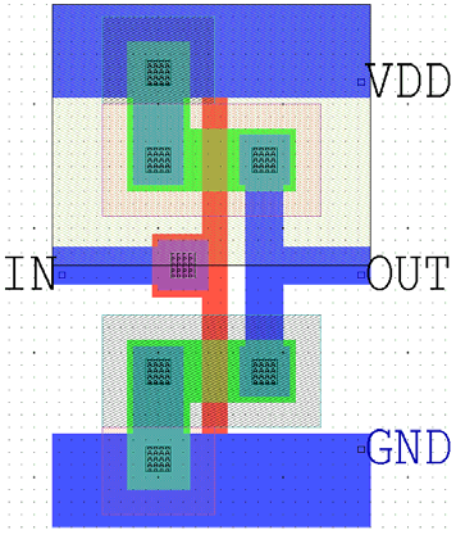
An Example of A Bad Layout



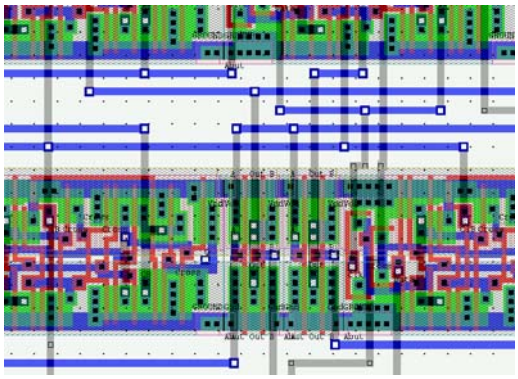
- **Not dense**
- **Long poly route (large parasitic resistance)**
- **Narrow power rails**

An Example of A Good Layout

- Very dense
- Short poly
- Wide power rails
- Both IN and OUT are in M1

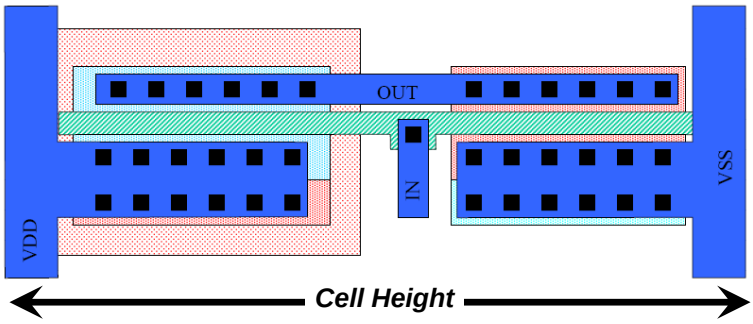


Channel Routing & Standard Cells



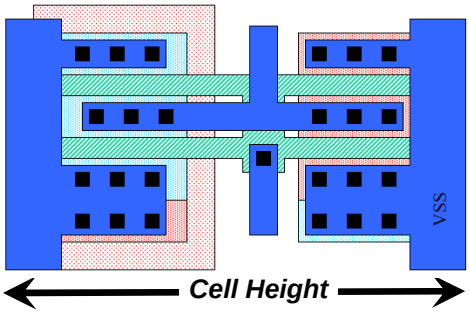
- All power and ground are connected nicely
  - This require that all cell height be the same for every cell
- M1 is used for horizontal routing in the channel
- M2 is used for vertical routing

Handling Large Device (Bad Layout)



- Long poly route (high resistance)
- Long source drain metal pickups (high resistance)
- Large cell height (mismatch with other cells)
- More component of diffusion cap then it needs to

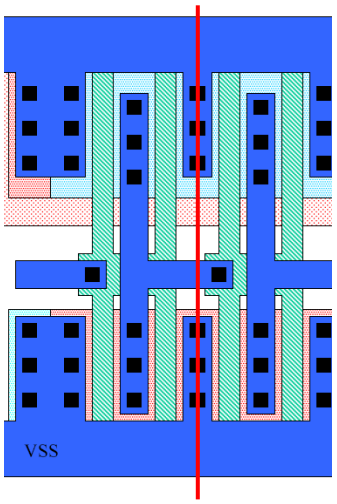
Handling Large Device (Good Layout)



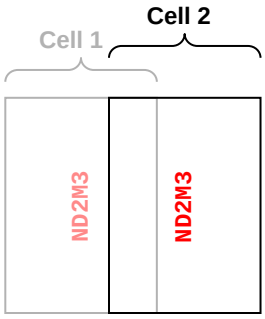
- The same drive strength (two folded transistor)
- Less diffusion capacitance (less P & A capacitance)
- Shorter poly route (lower resistance)
- Shorter source drain metal pickups (lower resistance)
- Smaller cell height (cab be matched with other cells)

Advantage of Folding Transistors

- Less poly and metal length
  - Lower parasitic resistance
  - Lower parasitic capacitance
- Less Drain periphery and area
  - Less diffusion capacitance (less C_{out})
- Less cell aspect ratio
  - Better match with other cells
  - More compact and faster circuit
- Both ends are VDD or GND
  - Can easily share the ends with neighbors

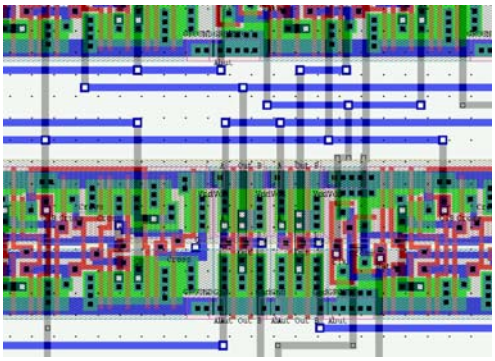


Overlapped Cells



- Our tools allow overlapping cells
  - This allows a cell to be complete and still share with the adjacent cell for better density
- This is why it is best to end cells on supplies
  - It is not possible to do always tough!

Random Logic Layout

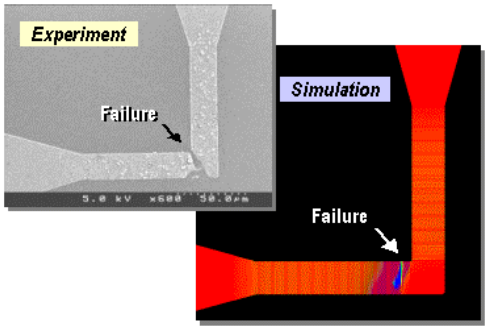


- Generally synthesized from an HDL description and automatically placed and routed (APR)
- Cells must be designed such that they line up nicely
- M1 is used for horizontal routing and M2 for vertical or vice versa

Layout Quality

- Electromigration (EM) and self-heating (SH) are the key reliability issues determined by layout
  - A quality layout will not limit the chip lifetime or speed
- Electromigration: Metal atoms swept out of position by "electron wind"
  - Only occurs on path where current flows in a single direction such as power supplies and between P and N devices
  - Depends on average current density
  - Highest at vias where the current crowds from the vias
- Self Heating: Long term failure of metal due to local IR heating
  - Occurs on wires with current flowing bidirectionally, eg, signal lines
  - Depends on I_{RMS}

Electromigration Modeling



- Using Physical models, we can predict where and when a failure can occurs
- By shrinking wire dimensions, electromigration is becoming more important
- Advanced VLSI technology will require checking the layout for electromigration as we do for DRC

Electromigration and Self-Heat

- Electromigration
  - Power Supply tracks
  - The track between PMOS and NMOS
  - Watch for "short circuit" current too
- Self-Heat
  - Output node wire
  - Can be large when C_L is large
- If the transistors are large, pre-determine the wire size and number of contacts and vias to prevent EM and SH