

# ECE321 – Electronics I

## Lecture 23: Logic Design Style: Static

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## *Review of Last Lecture*

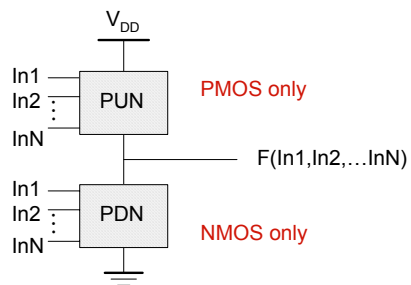
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- Transmission Gates**
  - Basic circuit for Transmission Gate
  - Circuit analysis Techniques
  - Complex Logic Gates using Pass Transistors

## Today's Lecture

- ❑ CMOS Static Gates
  - Implementation of a Complex Logic
  - Circuit Analysis for CMOS Static Gates
  - Transistor Sizing

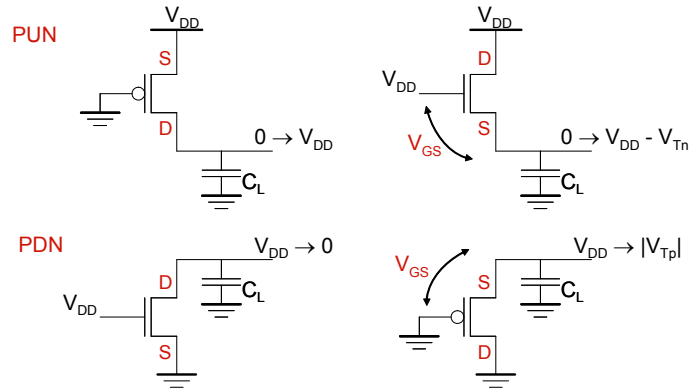
## Static CMOS Logic Gate



PUN and PDN are dual logic networks

- ❑ Static Logic is a gate where the output is maintained at 0 or 1 as long as power is applied
- ❑ PUN and PDN are dual (Complimentary) to drive the output from 0 to 1 and 1 to 0 full rail ( $V_{SS}$  to  $V_{DD}$ )

## PUN and PDN Networks

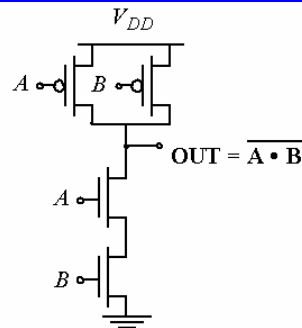


- NMOS is a good pull down device (PDN)
- PMOS is a good pull up device (PUN)

## Example: NAND Gate

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

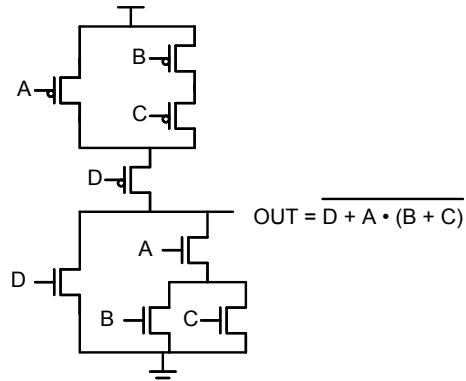


- PUN:  $\overline{A+B} = \overline{AB}$  (Conduction to VDD)
- PDN:  $AB$  (Conduction to GND)

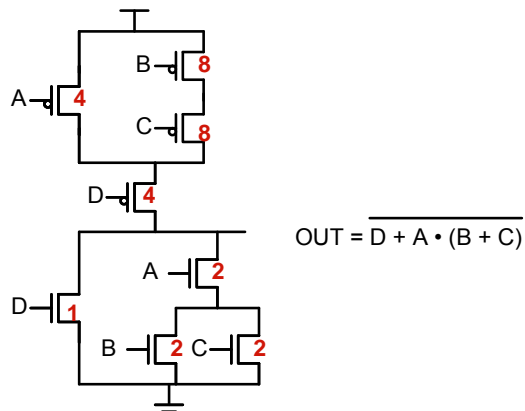
- How do you size transistors to have approximately the same delay as an inverter?

## Example: More Complicated Gate

- ❑ Consider  $F=D+A(B+C)$ 
  - Stacks give the AND function
  - Parallel gates give the OR function
- ❑ Derive the PDN in hierarchical fashion
- ❑ Build the complement for the PUN
  - Convert stacks to parallel
  - Convert parallel to stacks



## Transistor Sizing of a Complex CMOS Gate



- ❑ Size of transistors to have the same delay of an inverter when  $(W/L)_P=2$  and  $(W/L)_N=1$

## Circuit Analysis for Complex Gates

- To analyze complex gates for delay, power, and VTC, use the same concepts you have learned for inverter.
- Example: A CMOS gate with  $V_{DD}=5V$  is designed such that the base  $(W/L)=10$ . Assume that  $V_{Tn}=0.7$ ,  $V_{Tp}=-0.6$ ,  $K'_n=100 \mu A/V^2$ ,  $K'_p=60 \mu A/V^2$ , and the load capacitance is  $100fF$ . Use the constant current source model to find the best case and the worst case  $t_{pHL}$  and  $t_{pLH}$

