ECE321 – Electronics I

Lecture 24: Logic Design Style: Dynamic

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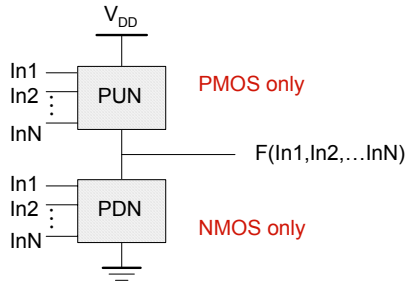
Review of Last Lecture

- **CMOS Static Gates**
  - **Implementation of a Complex Logic**
  - **Circuit Analysis for CMOS Static Gates**
  - **Transistor Sizing**

Today's Lecture

- **CMOS Dynamic Gates**
  - **Circuit Style**
  - **Pros and Cons**
  - **Charge Sharing Issue**

Static CMOS Logic Gate

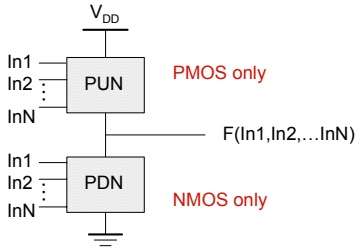


PUN and PDN are dual logic networks

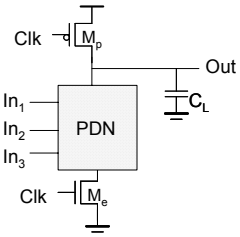
- **Static Logic is a gate where the output is maintained at 0 or 1 as long as power is applied**
- **PUN and PDN are dual (Complimentary) to drive the output from 0 to 1 and 1 to 0 full rail (VSS to VDD)**

Static versus Dynamic Logic Gate

Static Logic



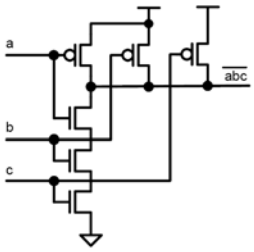
Dynamic Logic



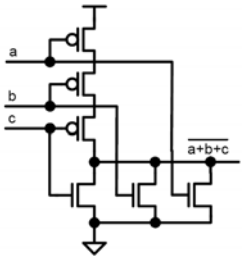
- Unlike static logic, in dynamic logic the output may leak away
- The output is valid only after pre-charge when clock applies

Issues with High Fan-in Static Logic

- Large number of devices (2x"fan-in"), which results in large C_L
- Large series stacks, which results in weak drive strength
- Wide devices, which results if large diffusion capacitance
- Large input capacitance, which is load to previous stage
- Large delay mostly due to large load capacitance



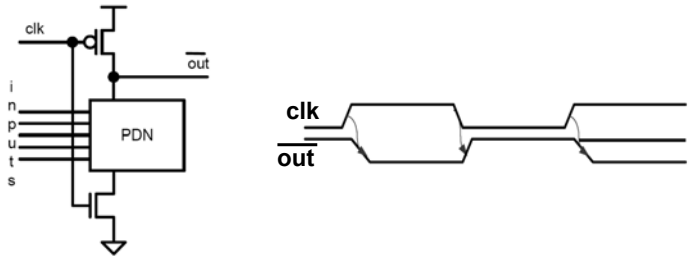
Example1: Static NAND3



Example2: Static NOR3

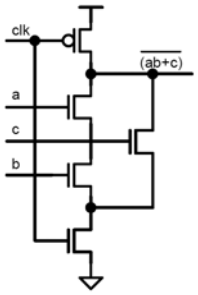
Introducing Dynamic Logic

- Fewer transistors ("fan-in"+2) since only PDN must be implemented
- PDN is comprised of NMOS, which is faster than PMOS
- t_{PLH} is essentially zero since the output is precharged
- Lower input capacitance since only NMOS is driven
- Low out put capacitance, which means very fast



Example: Implementation of a Function

- Example 1: Dynamic logic of $\overline{AB+C}$

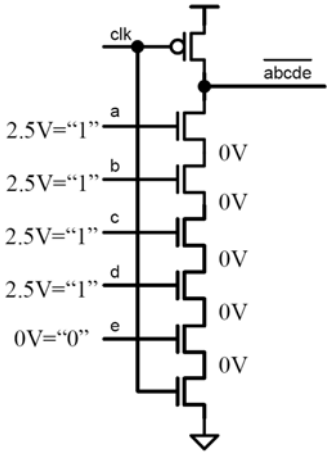


- Example 2: Dynamic logic of $\overline{(A+B)(C+D)}$

?

Charge Sharing (Problem 3)

- Charge sharing noise can discharge the output (dynamic) node



Previous inputs were such that the bottom of the stack was fully discharged. The next set of inputs were such that the output should be "1" but the inputs expose the output to enough diffusion capacitance that the charge sharing allows the output node to discharge anyways (at least to the V_{TH} of the following gate).

How to compute ΔV due to charge sharing?

Example: Compute Charge Sharing

The 3NAND dynamic gate is pre-charged, and then the top transistor M1 turns on. Given: V_{DD} = 1.5 V, V_{tn} = 0.4 V, C_L = 150 fF, C_1 = 25 fF, and C_2 = 50 fF. What is the final voltage?

Solution:

$$Q_{init} = C_L V_{DD} = 150\,fF \times 1.5V = 225\,fC$$

$$Q_{final} = Q_{init} = 225\,fC = C_L V_{final} + C_1 V_{final}$$

$$225\,fC = (150\,fF)(V_{final}) + (25\,fF)(V_{final})$$

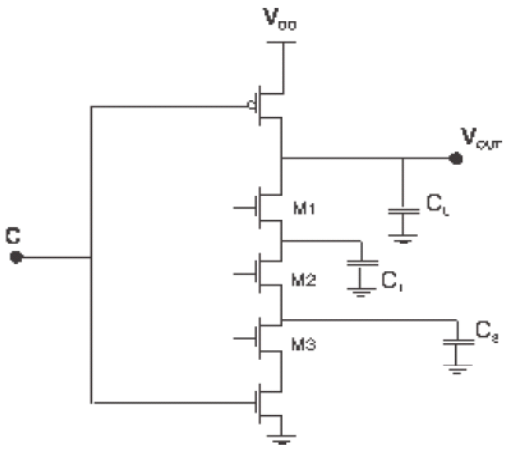
and

$$V_{final} = \frac{225\,fC}{175\,fF} = 1.286\,V$$

$$V_G - V_{tn} = 1.5 - 0.4 = 1.1\ \text{V}$$

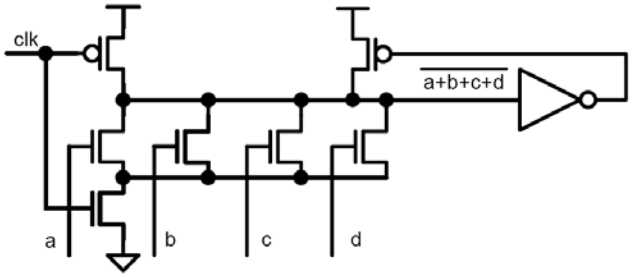
Q_1 = 1.1 V(25 fF) = 27.5 fF.

Then $V_{D1} = \frac{Q_{final}}{150\,fF} = \frac{225\,fC - 27.5\,fC}{150\,fF} = 1.317V$



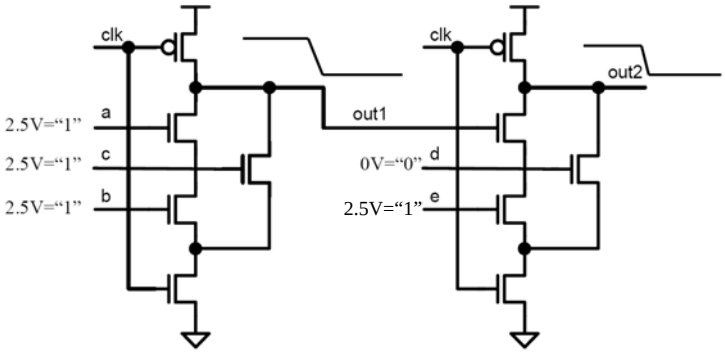
Solution to Charge Sharing

- Adding a PMOS keeper provides sufficient current to provide extra charge and eliminate the charge sharing problem
- This also increases the noise margin in general but slows down the gate. Why?



Cascading Gates (Another Problem)

- Domino gates cannot be directly attached to one another
- High to low transition is not allowed at any input



Out1 discharges on the evaluate phase, however it is pre-charged when the evaluate phase begins. Out2 is suppose to stay pre-charged. However since the M1 input (out1) is high during the first part of the evaluate phase is can partially or fully discharge.

Domino Logic (Solution)

- Cascaded gates must be buffered by static gates. This is called "domino" logic
- This eliminates the accidental discharge case by input high-to-low transition but also means that inverting domino gates can't be built