

ECE321 – Electronics I

Lecture 26: Timing Analysis

Payman Zarkesh-Ha

Office: ECE Bldg. 230B

Office hours: Tuesday 2:00-3:00PM or by appointment

E-mail: payman@ece.unm.edu

Review of Last Lecture

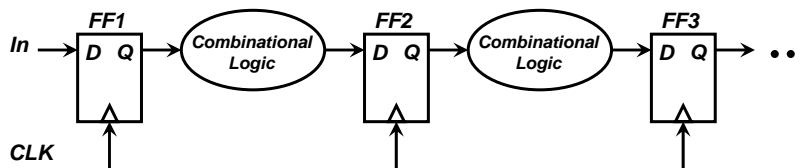
- Sequential Logic**
 - Latches and Flip-Flops
 - Timing Characteristics
 - Design of Latches and Flip-Flops
 - Setup and Hold Time Issues

Today's Lecture

- ❑ Timing Issues
 - Critical Path
 - Timing Constraints

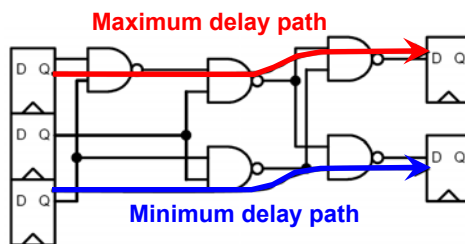
Pipelined Data path Circuit

- ❑ Flip flops synchronize data at each pipe stage start and finish
- ❑ Logic between them is combinational
- ❑ Since each stage begins and ends on a clock edge we can divide and conquer to determine the system timing
- ❑ This is called “timing analysis”



Timing Analysis

- ❑ Measure each path through the logic between FF's
- ❑ We really only care about the longest path, called maximum delay for setup
- ❑ Similarly, we only care about the shortest path, called minimum delay (or contamination delay) for hold
- ❑ The path that gives the maximum delay on the whole chip is called "critical path"



ECE321 - Lecture 26

University of New Mexico

Slide: 5

Minimum Clock Period

- ❑ Don't forget to consider delay of flip flops (setup, C2Q, and hold time) in maximum delay computation
- ❑ Example: Assuming that the setup time is 1ns, hold time is 1ns, and C2Q delay is 2ns, what is the minimum clock period? Why?



ECE321 - Lecture 26

University of New Mexico

Slide: 6

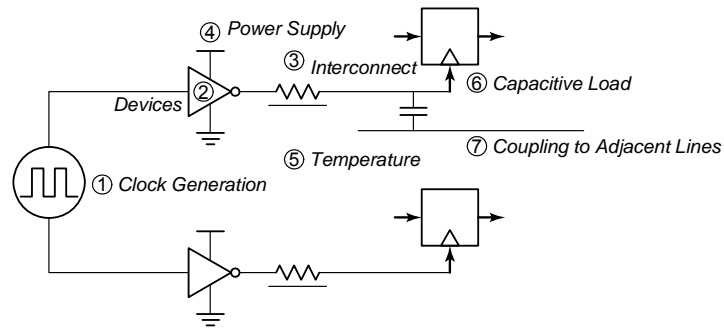
Clock Uncertainty

Clock skew

- Spatial variation in temporally equivalent clock edges; includes: deterministic + random

Clock jitter

- Temporal variations in consecutive edges of the clock signal; includes: modulation + random noise

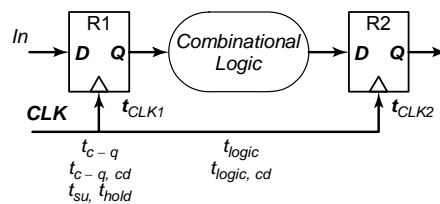


Clock Skew and Setup Time Constraint

Worst case is when receiving edge arrives early (positive δ)

Maximum delay is impacted since a clock cycle can be shorter than ideal

- Simply subtract the expected clock skew and jitter from the cycle time when designing
- A failure here is not too bad: It means that you missed a setup time
- The part is then “slow”—It will still work at a reduced clock rate



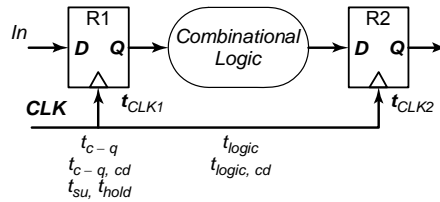
Minimum cycle time:

$$T - \delta = t_{c-q} + t_{su} + t_{logic}$$

$$\delta = t_{CLK1} - t_{CLK2}$$

Clock Skew and Hold Time Constraint

- ❑ Worst case is when receiving edge arrives late, (positive δ)
- ❑ Minimum delay is impacted since a receiving clock edge can be later than ideal
 - Means that the hold time at the receiving latch is more easily violated
 - A failure here is pretty much catastrophic
 - Since skew is built-in, there is nothing you can do post-silicon to fix it!
 - It is generally worth-while to add more design guard-band (margin) to your min-delay timing!

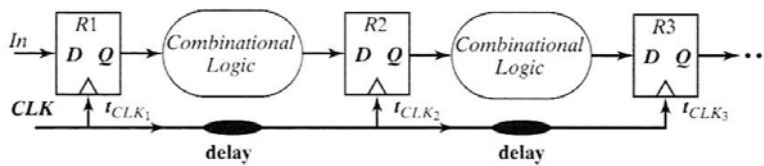


Hold time constraint:

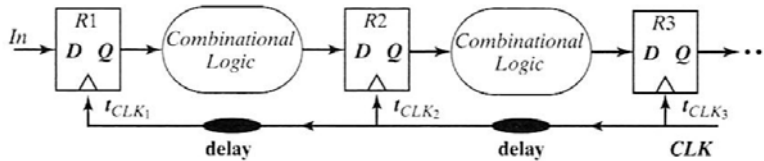
$$t_{(c-q, cd)} + t_{(logic, cd)} > t_{hold} + \delta$$

$$\delta = t_{CLK2} - t_{CLK1}$$

Positive and Negative Skew



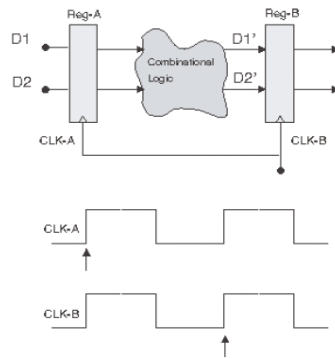
(a) Positive skew



(b) Negative skew

Example: Timing Constraints

How fast can the circuit in Fig. 8-23 be clocked if $t_{su} = 2 \text{ ns}$, $t_{hold} = 3 \text{ ns}$, $t_{logic} = 15 \text{ ns}$, $t_{logic-cd} = 11 \text{ ns}$, and $t_{cq} = 4 \text{ ns}$.



$$T > t_{cq} + t_{logic} + t_{su} = (4 + 15 + 2) \text{ ns} = 21 \text{ ns}$$

$$F_{MAX} = \frac{1}{T} = \frac{1}{21 \text{ ns}} = 47.62 \text{ MHz}$$

Another Example: Effect of Clock Skew

- Assume $t_{C2Q} = 350 \text{ ps}$ and $T_{hold} = 100 \text{ ps}$. What happens?
- Assume $t_{C2Q} = 150 \text{ ps}$ and $T_{hold} = 100 \text{ ps}$. What happens?

