

ECE321 – Electronics I

Lecture 27: SRAM Memories

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Review of Last Lecture

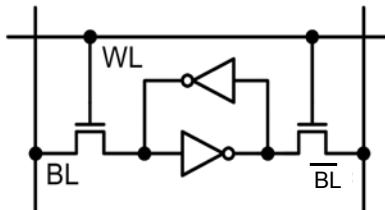
- Timing Issues**
 - Critical Path
 - Timing Constraints

Today's Lecture

- ❑ Static Random-Access Memory (SRAM)
 - SRAM cell
 - SRAM architecture
 - Sense amplifier

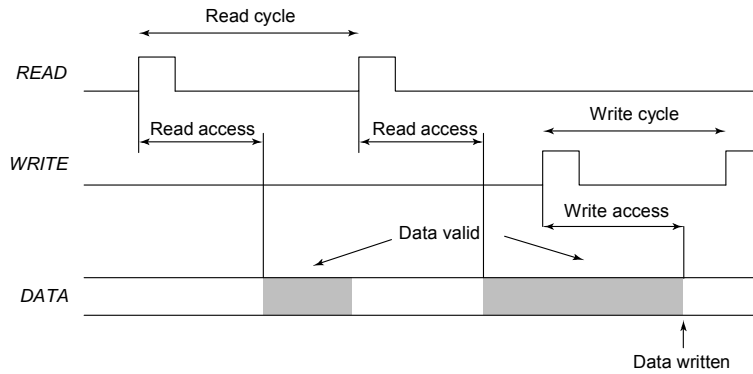
SRAM Cell

- ❑ SRAM cell is quite similar to flip-flop without any protective circuitry
- ❑ Therefore, reliable operation imposes transistor sizing constraints.
- ❑ Cell is selected by word line ($WL=1$) and read and write are often differential



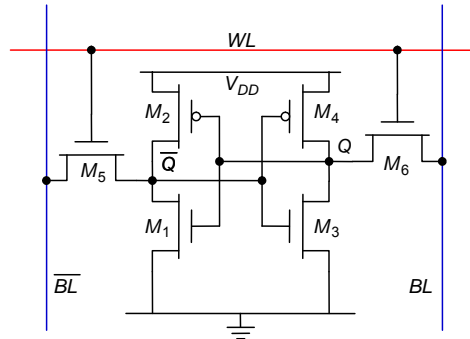
Memory Read and Write Timing

- ❑ Memory timing parameters includes: *read-access time, write-access time, read-cycle time, and write-cycle time*



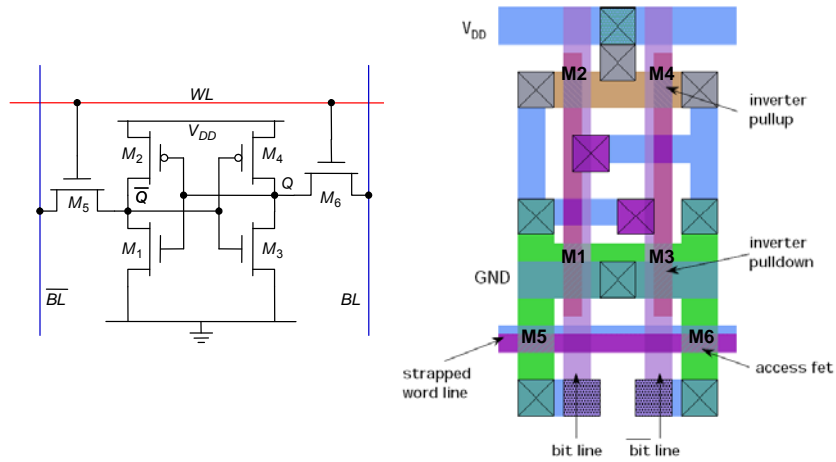
6-T SRAM Cell

- ❑ SRAM cell consists of 6 transistors (6T cell) with differential BL
- ❑ When reading, BLs are at VDD and have high capacitance
 - This is essentially a short to VDD for both side of the cell
 - The side at logic one is unaffected. e.g. Q at VDD and BL at VDD
 - Node \bar{Q} is pulled up by the voltage divider of two NMOS transistors



SRAM Layout

- Layout must be symmetric to reduce process variation



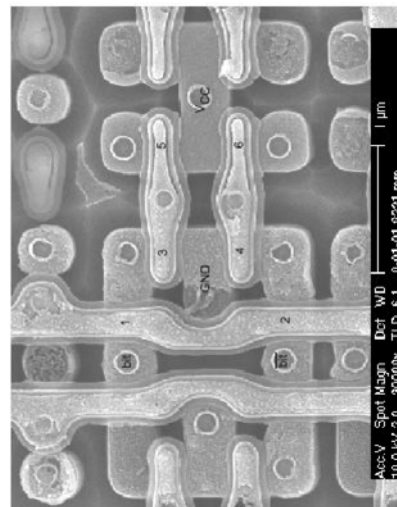
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Real SRAM Cell

- Real cells will have extensive corner rounding and layer misalignment
 - Hence the cell will not be symmetric in reality
 - Note rounding and misalignment!
- Since there are a lot of statistics in a large SRAM, e.g., 1MB L2 has nearly 10M cells (including ECC) so random variation will work against full yield
 - This can be partly made up by redundancy
 - But solid cell design is essential
 - Worst case process corners must be used



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SRAM Read - Sensing

- ❑ The simplest reading is an inverter sense
 - This is slow unless the BL is very short
- ❑ Generally, we want to use a sense amplifier
 - Smaller swing on BLs (only about 50mv is necessary)
 - The SRAM cell transistors are small and weak and BL has high capacitance. Therefore, BL swing is very slow. Faster operation requires smaller swing.
 - Smaller swing saves power (as long as we don't drive the BLs with the sense amplifier) by limiting swing on the BLs

Sense Amplifier : Static

- ❑ A simple OPAMP can be used as sense amplifier
 - Unfortunately in practice, it is very slow to respond
 - This is static, since the output is only as a function of input
- ❑ This circuit has serious CMRR problems, particularly when both inputs are near the VDD rail

