ECE321 – Electronics I

Lecture 28: DRAM & Flash Memories

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Review of Last Lecture

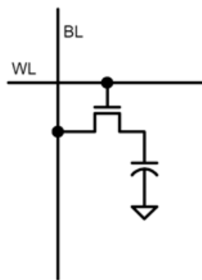
- **Static Random-Access Memory (SRAM)**
  - **SRAM cell**
  - **SRAM architecture**
  - **Sense amplifier**

Today's Lecture

- Dynamic Random-Access Memory (DRAM)
  - DRAM cells
  - DRAM Capacitor implementation
  - DRAM Sense amplifier
- Nonvolatile Memories
  - EPROM
  - EEPROM
  - Flash

1T DRAM Cell

- Stored bit is held dynamically on a capacitor
- Very small storage cell – only 1 transistor
  - Originally the capacitance was just the drain capacitance
- Unfortunately, charge doesn't scale – key to technology is packing more capacitance into a smaller area over time
  - Tow main approaches: (1) Trench capacitor, (2) stacked capacitor

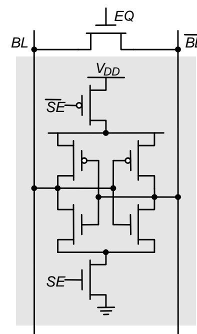


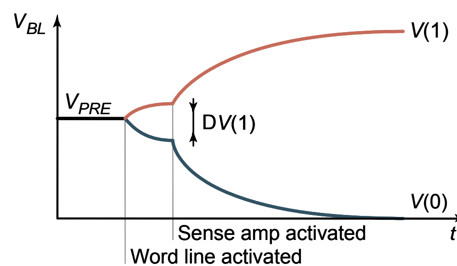
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than VDD

Sense Amplifier in DRAM

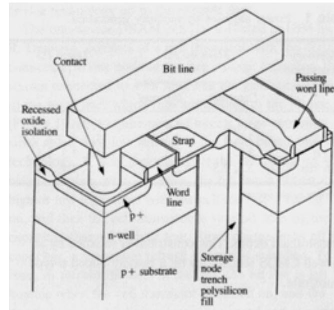
- sense amp enabled with SE
- Initialized in its meta-stable point with EQ
- Once adequate voltage gap created, positive feedback quickly forces output to a stable operating point

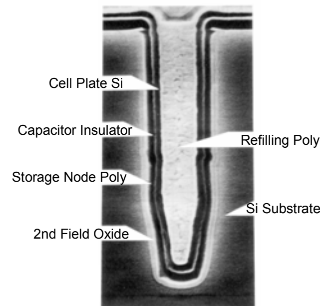




DRAM Technology – Trench Capacitor

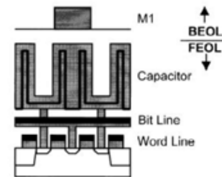
- Capacitor is the trench under select line
- The sidewalls and bottom of the trench are used for capacitor
- Trench is up to 5um deep

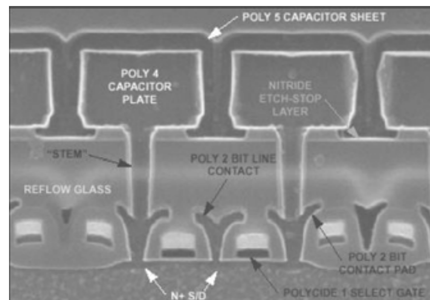


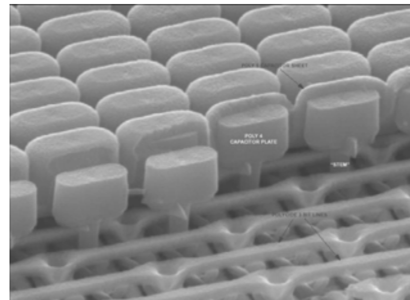


DRAM Technology – Stacked Capacitor

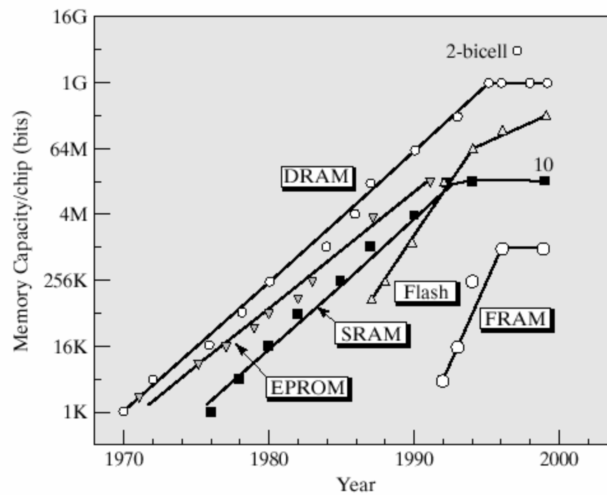
- Capacitor is above select transistor
- Polysilicon vias to polysilicon Plates





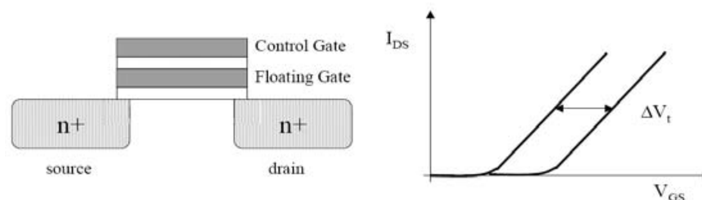


Semiconductor Memory Trends



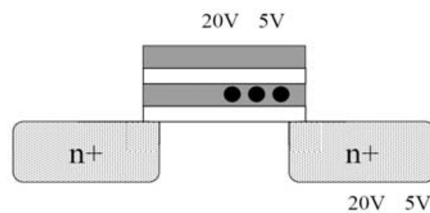
Nonvolatile Memories

- All present non-volatile memories are based on ROM memory configurations
  - All retain the single BL, although the sensing may be differential, using comparison to some reference voltage or replica BL
- The key to present memories is the ability to change the V_T of the transistor by adding or removing charge from a floating gate



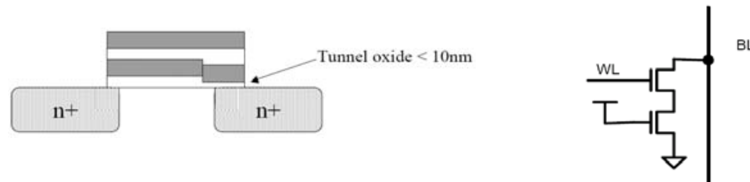
Erasable Programmable ROM (EPROM)

- ❑ Uses the same ROM NOR topology but can electrically increase the V_T of a cell via hot electron injection to a floating gate
- ❑ Erase is by UV light: Energetic photons knock the charge off the floating gate
  - This is an off-line operation and requires expensive packages with windows
  - Windowless packages are used for one time program (OTP)



Electrically Erasable PROM (EEPROM)

- ❑ EEPROM allows electrical erase of the cells
  - By providing a thin oxide at the drain end, the proper voltage can remove the charge via Fowler-Nordheim tunneling
  - The cells require two transistors per cell however
- ❑ A drawback of this cell is V_T drift when exposed to read voltages A separate access transistor helps to alleviate this problem, but at a significant density penalty



Flash Memories

- Flash memories also allow electrical erase but at better granularity and speed
- A single thin oxide is used and a one transistor cell is possible
- Flash is available in NOR and NAND varieties
  - Flash is faster so can be main memory - still very slow compared to SRAM
  - It is impractical to directly run code from NAND so it is primarily popular as data storage, e.g., photos, USB drives, etc.
- Multiple level cells are possible with choices of 4 V_Ts
  - This requires multiple sense amplifiers or multiple passes
  - Programming precise values is difficult and “over-erase” must be avoided
- Scaling flash transistors is very difficult since the oxide cannot scale
  - About 1 electron per month is the allowable loss