University of New Mexico
Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2013) **Exam 1**

Name: Solutions Date: November 11, 2013

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) True or false:

(a) Drain potential in NMOS is always lower than the Source potential. (F)

(b) Based on DIBL effect, the threshold voltage of an NMOS increases by decreasing Drain potential. (T)

(c) It is always desirable to have larger noise margin. (T)

(d) In a CMOS inverter, the NMOS is responsible for low-to-high transition. (F)

(e) The unit of channel length modulation factor, λ, is V^{-1}. (T)

2. (10 points) The minority carrier concentration in a doped silicon wafer at room temperature is n_0=1000 electrons/cm^3. Assume that n_i=1.062x10^{10} electrons/cm^3.

(a) Determine the type of semiconductor (N or P type)

(b) Calculate the majority carrier concentration.

(c) Find the doping concentration.

d (e) What is the minority carrier concentration at 0 ºK?

a) P type

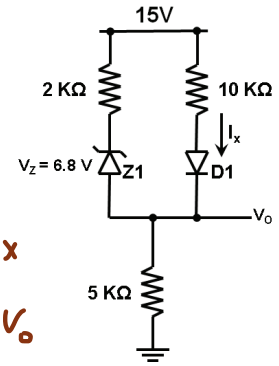
b) $nP = n_i^2 \Rightarrow P = (1.062\times10^{10})^2 / 1000 = 1.127\times10^{17}$ holes/cm^3

c) $N_A \approx P = 1.12\times10^{17}$ atoms/cm^3

d) $n\,(@\,T=0^{\circ}K) = 0$

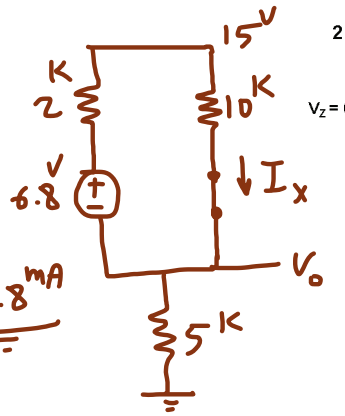
3. (20 points) Assume that D1 is an ideal diode and the Zener diode Z1 has V_Z=6.8V. Determine I_X and V_O.

Assume: { D: Forward; Zener: Breakdown



KCL:

$$\frac{V_o - 15}{10K} + \frac{V_o - (15-6.8)}{2K} + \frac{V_o}{5K} = 0$$



$\Rightarrow V_o = 7^V \Rightarrow I_x = \frac{15-7}{10K} = 0.8^{mA}$

$I_x > 0 \Rightarrow D_1$: Forward ✓

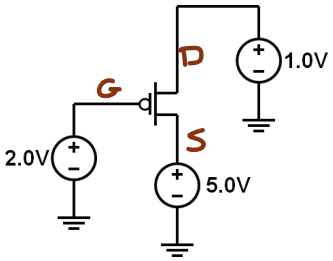
$I_z = \frac{15-6.8-7}{2K} = 0.6^{mA} > 0 \Rightarrow$ Zener : Breakdown ✓

4. (20 points) In the circuit below, assume that the PMOS has K'_p=60uA/V^2, (W/L)=10, and V_{tp}=-1V. Ignore the body effect and channel length modulation.

(a) Identify Source, Gate, and Drain terminals

(b) Find the region of operation

(c) Determine I_{DS}



b) $|V_{DS}| \;?\; |V_{GS}| - |V_{Tp}|$

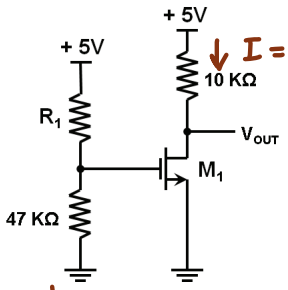
$4^V > 3^V - 1^V$

$\Rightarrow$ Saturation

c) $|I_{DS}| = \frac{K'_p}{2}\left(\frac{W}{L}\right)\left(|V_{GS}| - |V_{Tp}|\right)^2$

$= \frac{60^{\mu A/V^2}}{2} \times 10 \times (3-1)^2 = 1.2^{mA} \Rightarrow I_{DS} = -1.2^{mA}$

5. (20 points) In the following circuit find R_1 such that V_{out}=2.5V. Let V_{Tn}=1V, K'_n=100 μA/V^2, and (W/L)=10.



Assume Saturation:

$I_{DS} = I = 0.25\ mA$; $I_{DS} = \frac{K'_n}{2}\left(\frac{W}{L}\right)(V_{GS}-V_T)$

$\Rightarrow 0.25\ mA = \frac{100\ mA/V^2}{2} \times 10 \times (V_{GS}-1)^2 \Rightarrow V_{GS} = 1.7\ V$

$I = \frac{5-2.5}{10K} = 0.25\ mA$

Voltage Division : $5 \times \frac{47^K}{R_1+47^K} = 1.7^V \Rightarrow R_1 = 90.6\ k\Omega$

V_{DS} ? $V_{GS}-V_T$

$2.5^V > 1.7-1 \Rightarrow$ Saturation ✓

6. (20 points) Determine the maximum load capacitance in a CMOS inverter, such that the maximum low-to-high propagation delay, t_{pLH}, is limited to 500ps. Assume that the PMOS transistor stays in saturation during the entire transition. Let V_{DD}=5V, V_{Tp}=-1V, K'_p=60 μA/V^2, and $(W/L)_p$=20.

$t_{PLH} = \frac{C_L \Delta V}{I_{av}}$: $\frac{C_L \times (V_{DD}/2)}{\frac{K'_p}{2}\left(\frac{W}{L}\right)(V_{DD}-|V_{Tp}|)^2} = t_{PLH}$

$\Rightarrow \frac{C_L \times 2.5}{\frac{60\ mA/V^2}{2} \times 20 \times (5-1)^2} < 500^{PS} \Rightarrow C_L < 1.92^{PF}$