ECE 338 - Advanced Logic Design  
Spring 2010

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Office: ECE 230C  
Office Hrs: Mon 9:00 to 11:00 AM; Wed 1:30 to 3:30 PM  
(Other times by appointment)

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This book forms part of the presented material. In addition, you will need to take copious notes, and from time to time handouts will be given in class. Information will also be made available on the departmental computers.

Additional information available at:  http://www.ece.unm.edu/faculty/pollard

Computer information: will need account on the ECE departmental systems. This will be used for Mentor Graphics suite schematic capture and simulation, as well as the use of VHDL for system representation. You are free to use whatever document preparation system you prefer for your reports.

Topics:
- Introduction to computer aided design (CAD): schematic capture systems, simulation systems, design languages, and system integration.
- Advanced combinational circuits: look-ahead techniques, parallel multipliers, dividers, shift networks, parity trees; floating point hardware designs.
- Information representation: theory and practice of value representation and manipulation.
- Use of Register Transfer Languages (RTL) and Hardware Description Languages (HDL) in the design process.
- Sequential design methodologies: delay line methods, shift register methods, and state machine methods.
- Programmable Logic Devices: design with registered and combinational PLDs and FPGAs.
- Asynchronous sequential design. Timing issues: set up, hold, clock to Q, clock skew, transition time, pulse width.
- Hazards: static 0, static 1, dynamic 0, dynamic 1, essential, gated clocks. Races, loops, oscillations.
- Memories and memory interfacing: SRAM, DRAM, (E(P))ROM, Flash, etc.

Required work: There will be three or four design assignments. The design assignments are non-trivial; plan to spend time on them.

Grading: (Current iteration of...)
- Design Assignments: 40 %
- Hour Exams (2): 30 %
- Final Exam: 30 %

Additional Reading and References: