Memory Scrubber System

FPGA = The Brains

Memory = UUT

Address
Control
Data
**Functional Activities**

- Fill the memory with pattern (= Address)
- Read a memory location
- Restore data to the memory location
- Loop through all addresses

**Memory = 256K x 32**

- Address lines (17..0)
- Data lines (31..0)
- Control lines (asserted LOW)
  - CE – Chip Enable
  - OE – Output Enable
  - UB, LB – Upper/Lower Byte Enable
  - WE – Write Enable
FPGA Data Path Block Diagram

- **Clear, Inc**: ADDRESS
- **Load**: DATA_REG
- **TSD**: ADDRESS

State Diagram (1)

- **Start**
  - (wait)
  - Write Val Inc Addr
  - check for done
- **Read Mem (to Reg)**
  - (wait)
  - Write Val Inc Addr
  - (wait)
State Diagram (2)

S0: ADDR <= 0
S1: (wait)
S2: WE, UBE, LBE, CE
   ADDR++
S3: ADDR /= 0
S4: CE, UBE, LBE, OE, REG_EN
S5: (wait)
S6: WE, UBE, LBE, CE, REG_OE
   ADDR++
S7: (wait)

Expected Waveforms

Clock

CE, UBE ...

Address/Data