1. (10 points) True or false:
   (a) In a CMOS inverter, the maximum short circuit current occurs when the input voltage is at the switching threshold voltage. (T)
   (b) By definition, \( V_{IL} \) is maximum input voltage of a logic gate that still can be detected as zero. (T)
   (c) The dynamic power in a CMOS inverter is the amount of power that is consumed in the load capacitor. (F)
   (d) To have a better noise margin in logic gates, it is better to maximize \( V_{OH} \) and minimize \( V_{IH} \). (T)
   (e) In a CMOS inverter, reducing the NMOS threshold voltage, \( V_{th} \), reduces the low-to-high propagation delay, \( t_{PLH} \). (F)

2. (15 points) Compute the leakage power consumption in a CMOS inverter that is used in a clock distribution network of a digital circuit using 90nm technology node. Assume that the \( V_{DD} \) is 1.2 V, \( I_{OFF(NMOS)} \) = 12 nA/\mu m, and \( I_{OFF(PMOS)} \) = 26 nA/\mu m, \( (W/L)_n \) = 650, \( (W/L)_p \) = 950, and L = 90nm.

\[
P_{\text{leakage}} = \frac{1}{2} V_{DD} \left( I_{\text{off(nmos)}} + I_{\text{off(pmso)}} \right)
\]

\[
W_n = 58.5 \mu m \quad I_{\text{off(nmos)}} = 702 \text{nA}
\]

\[
W_p = 85.5 \mu m \quad I_{\text{off(pmso)}} = 2223 \text{nA}
\]

\[
P_{\text{leakage}} = \frac{1}{2} \times 0.5 \times (702 \text{nA} + 2223 \text{nA}) = 1.755 \mu W
\]
3. (20 points) You are given two digital systems, A and B, and are asked to connect the outputs of system A to the inputs of system B. The power supply voltage for system B is 1.5V, but the power supply voltage of system A is slightly less; at 1.2V.

(a) Assume that all the logic gates inside systems A and B can be treated as CMOS inverters. Determine $V_{OH}$ and $V_{CL}$ for the outputs of system A?

(b) For the system B, assume that $V_{IL}=0.2$ and $V_{IH}=1.3$. Draw the noise margin map and compute NMH and NML.

(c) Explain why the overall system won't work.

a) For CMOS inverters operation is "rail-to-rail."

\[ V_{OH} = V_{DD} = 1.2V \quad V_{CL} = 0V \]

b) System A

\[ 1.2V \quad V_{OH} \]

\[ 0V \quad V_{CL} \]

System B

\[ V_{IH} \quad 1.3V \]

\[ V_{IL} \quad 0.2V \]

\[ N_{MH} = V_{OH} - V_{IH} = 1.2 - 1.3V = -0.1V \]

\[ N_{ML} = V_{IL} - V_{CL} = 0.2V - 0.0V = 0.2V \]

c) The maximum output of A is below the minimum input for high logic of system B. When A tries to communicate a logic high, it will appear as undefined logic to system B.
4. (30 points) We would like to design an inverter to drive a long interconnect (clock line) with effective capacitance of 10 pF. By computing the average current that charges/discharges $C_L$, determine $\frac{W}{L}_P$ such that $t_{PLH} = 250$ ps. Assume that $V_{DD} = 2.5V$, $V_{DD} = -0.4 V$, and $K' = -60 \mu A/V^2$.

\[ I_{AV} = \frac{1}{2} \left[ I \left( V_{in} = 0 \land V_{cut} = 0 \right) + I \left( V_{in} = 0, V_{cut} = \frac{V_{dd}}{2} \right) \right] \]

\[ I_{AV} = \frac{1}{2} \left[ \frac{1}{2} \frac{k_p}{C_L} \left( \frac{W}{L}_P \right)^3 (V_{DD} - V_{thP})^3 + \frac{K'}{C_L} \left( \frac{W}{L}_P \right)\left( (V_{DD} - V_{thP}) \frac{V_{DD}}{2} - \frac{W_{dd}^2}{8} \right) \right] \]

\[ I_{AV} = \frac{1}{2} \left[ 1.325 \times 10^{-4} \left( \frac{W}{L}_P \right)^3 + 1.106 \times 10^{-4} \left( \frac{W}{L}_P \right) \right] = 1.215 \times 10^{-4} \left( \frac{W}{L}_P \right) \]

\[ t_{PLH} = \frac{C_L \times \frac{V_{dd}}{2}}{I_{AV}} \rightarrow 250 \mu s = \frac{10 \text{ pF} \times 1.25V}{I_{AV}} \rightarrow \left( \frac{W}{L}_P \right) = \frac{411.65}{2} \]
5. (25 points) In an ideal CMOS inverter, $V_{OH}$ is equal to $V_{DD}$. However, the NMOS leakage may slightly reduce $V_{OH}$. In this problem, we want to calculate the $V_{OH}$ in the presence of NMOS leakage. To measure $V_{OH}$, you connect the input to the ground, where the PMOS is in linear region and the NMOS is in cutoff region. However, in the presence of leakage, you can approximate that the NMOS behaves like a current source with the current of $I_{OFF(NMOS)}$ as shown in the circuit below. Compute $V_{OH}$, if $I_{OFF(NMOS)}=1 \mu A$, $V_{DD}=1.0 \text{ V}$, $V_{lp}=-0.4 \text{ V}$, $K_p\quad = -40 \mu A/V^2$, and $(W/L)_p=2$.

\[ I_{off,n} = |K_p| \left( \frac{W}{L} \right)_p \left[ (V_{dd} - V_{th}) (V_{dd} - V_{oh}) - \frac{(V_{dd} - V_{oh})^2}{2} \right] \]

\[ I_{\mu A} = 10 \mu A \times 2 \times \left[ (1 - 0.4) (1 - V_{oh}) - \frac{(1 - V_{oh})^2}{2} \right] \]

$V_{OH} = 0.9787 \text{ V}$