1. (10 points) Fill in the blank:
   (a) In standard CMOS process, the source and drain are formed by using _______________ layer masks.
   (b) The process of manufacturing transistors is called _______________ and the process of manufacturing interconnects is called _______________.
   (c) CMP stands for _____________________________.
   (d) The effective width of two series NMOS with $W_1=6\mu$m and $W_2=3\mu$m is ______.
   (e) Electromigration is _____________________________.

2. (20 points) You are asked to layout the power and ground bus in the layout of a logic block in a real chip. Assume that the logic block draws 80mA of current and the metal thickness is 0.4 um. If the maximum current density $J_{\text{max}} = 2\times10^6 \text{ A/cm}^2$, determine the minimum width (in micron) of the interconnect that is needed to power the logic block.
3. (30 points) A three-input CMOS NAND gate is designed as shown below. Assume that \( V_{DD}=1.2 \text{ V} \), \( K'_n=90 \mu\text{A/V}^2 \), \( V_{tn}=0.4 \text{ V} \), \( K'_p=50 \mu\text{A/V}^2 \), and \( V_{tp}=-0.5 \text{ V} \) in the 100nm technology node.

(a) Determine the width of NMOS and PMOS transistors in this NAND gate, such that the worst case delay becomes equivalent to a referenced inverter with \( W_n=1\mu\text{m} \) and \( W_p=2\mu\text{m} \).

(b) For the device sizes found in part (a), determine the switching threshold voltage, \( V_M \), when all inputs are tied together.

(c) Find the maximum \( I_{DD} \) current for this NAND gate.
4. (40 points) We would like to design the following circuit such that the worst case propagation delays \((t_{pHL} \text{ and } t_{pLH})\) are limited to 2.14 ns. Use Elmore delay equation to determine the W/L for PMOS and NMOS used in the 3-input NAND gate. Assume that \(V_{DD}=1.2\ V\), \(K'_n=90\ \mu A/V^2\), \(V_{th}=0.4\ V\), \(K'_p=50\ \mu A/V^2\), and \(V_{tp}=-0.5\ V\) in the 100nm technology node. Also assume that the transistors stay in saturation region for the length of the transition.