Lecture 17: Interconnect Modeling I

Review of Last Lecture

- Gate Sizing (Inverter Chain)
Today’s Lecture

- Interconnect Resistance
- Interconnect Capacitance
- Interconnect Inductance

Interconnect Modeling

- Interconnect parasitics
  - reduce reliability (crosstalk noise)
  - affect performance and power consumption

- Interconnect Modeling
  - Parasitic Capacitance
  - Parasitic Resistance
  - Parasitic Inductance
Example: Intel 0.25μm backend process

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

<table>
<thead>
<tr>
<th>LAYER</th>
<th>PITCH</th>
<th>THICK</th>
<th>A.R.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>0.67</td>
<td>0.40</td>
<td>-</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>0.64</td>
<td>0.25</td>
<td>-</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.84</td>
<td>0.48</td>
<td>1.5</td>
</tr>
<tr>
<td>Metal 2</td>
<td>0.93</td>
<td>0.90</td>
<td>1.9</td>
</tr>
<tr>
<td>Metal 3</td>
<td>0.93</td>
<td>0.90</td>
<td>1.9</td>
</tr>
<tr>
<td>Metal 4</td>
<td>1.60</td>
<td>1.33</td>
<td>1.7</td>
</tr>
<tr>
<td>Metal 5</td>
<td>2.56</td>
<td>1.90</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Layer pitch, thickness and aspect ratio

Interconnect Resistance

- Extraction of interconnect capacitance is simpler except for special cases (test chips where accurate resistance of a pattern is needed)
- Sheet resistance is an easy method of resistance measurement in layout (Only the metal aspect ratio is needed, no thickness information)

\[ R = \frac{\rho L}{WH} \]

Sheet Resistance
Example: Interconnect Resistance

If the line is made of Cu, calculate the line resistance using sheet resistance at \( T = 20°C \).

The sheet resistance is 
\[ R_{\text{sheet}} = \frac{\rho}{r} = \frac{1.72 \, \mu\Omega \cdot \text{cm}}{0.5 \, \mu\text{m} / \text{cm}} \times \frac{10 \, \mu\text{m}}{\text{cm}} = 33.99 \, \text{m\Omega/square} \]

And the total number of squares is \( \frac{1}{w} = 10 \, \mu\text{m} / 0.25 \, \mu\text{m} = 40 \) squares. The total resistance is then

\[ R = 33.99 \, \text{m\Omega} \times 40 = 1360 \, \Omega \]

You get the same result from Eq (1), but deal with one less constant in the sheet resistance calculation.

Sheet Resistance

- Measurement shows that the effective number of squares of the “dog bone” style contact region is 0.65 and for a 90° corner is 0.56
Interconnect Capacitance

- Extraction of interconnect capacitance in modern VLSI technology is very complicated because of
  - Non-homogenous dielectric (etch stop, barrier liner, etc.)
  - Complex pattern of neighboring interconnects (need 3D modeling)

- There are two types of capacitances:
  - Ground capacitances
  - Coupling capacitances

Interconnect Capacitance Modeling

- Often simple parallel plate model is used for hand calculation

\[ C_{eq} = \frac{\varepsilon_{di} WL}{t_{di}} \]

Example:
Consider the static situation in the figure where line-1 is at 1.5 V and line-2 is floating. What is the induced voltage on line-2?

\[ V_2 = \left[ \frac{10}{10 + 2} \right] \times (1.5\,\text{V} - 1.0\,\text{V}) = \frac{5}{12} \times 0.5\,\text{V} = 0.208\,\text{V} \]
**Interconnect Inductance**

- Extraction and modeling of interconnect inductance is extremely hard because of:
  - Non-identified return path
  - Unlike capacitance, the effect of inductance goes beyond nearest neighbors
- It is used only for specific nets such as clock and power supply interconnects
- Has not yet been used by industry for timing analysis

**Example: Inductance in Power Supply**

The inductance in a particular IC connecting metal is 200 pH. What is the inductive voltage generated during a current rise time of 10^7 A/s?

\[ v_L = L \frac{di}{dt} = 200 \times 10^{-12} \times 10^7 = 200 \text{ mV} \]

Many ICs use power supply voltages on the order of 1.0 V and less. A 200 mV inductive rise is a severe temporary weakening of the normal voltage that drives logic circuitry.
Dealing with Interconnect Parasitics

- Reduce interconnect Capacitance
  - Use better dielectric material (low-K dielectric)
  - Reduce wire-length (efficient layout)
  - Increase wire spacing

- Reduce Interconnect Resistance
  - Use better conductor material (Copper)
  - Reduce wire-length (efficient layout)
  - Increase wire width

- Reduce Interconnect Inductance
  - Use proper return path
  - Slow down the ramp time