Review of Last Lecture

- Interconnect Resistance
- Interconnect Capacitance
- Interconnect Inductance
Today’s Lecture

- Miller Effect
- Interconnect Delay
- Elmore Delay

Interconnect Complexity

- Interconnects are getting more complex as technology improves
- Current technology can have 12 layers of metal ranging from 1um to 10,000um length
- Wire pitch is 90nm for 45nm technology node

<table>
<thead>
<tr>
<th>Technology</th>
<th>65 nm (now)</th>
<th>45 nm (2008)</th>
<th>32 nm (2010)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire width</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
</tr>
<tr>
<td>Wire Thickness</td>
<td>115 nm</td>
<td>80 nm</td>
<td>60 nm</td>
</tr>
<tr>
<td>Total Number of Wires</td>
<td>60 Million</td>
<td>150 Million</td>
<td>300 Million</td>
</tr>
<tr>
<td>Total wire length</td>
<td>1 mile</td>
<td>1.4 mile</td>
<td>2 mile</td>
</tr>
</tbody>
</table>
Effective Capacitance & Miller Effect

- If \( W_1, W_2, W_3, \) and \( W_4 \) are grounded (not switching), then the total capacitance that the \( W_x \) wire sees is:
  \[ C_x = C_1 + C_2 + C_3 + C_4 \]
- If \( W_2 \) and \( W_4 \) are grounded but \( W_1 \) and \( W_3 \) switches in the **same direction** of \( W_x \), then the total capacitance that the \( W_x \) wire sees is:
  \[ C_x = C_2 + C_4 \]
- If \( W_2 \) and \( W_4 \) are grounded but \( W_1 \) and \( W_3 \) switches in the **opposite direction** of \( W_x \), then the total capacitance that the \( W_x \) wire sees is:
  \[ C_x = 2C_1 + C_2 + 2C_3 + C_4 \]

Interconnect Time Constant & Delay

- Interconnect circuit can be simplified as an RC network.
- The time constant of an interconnect is simply \( \tau = RC \)
- However, the propagation delay of an RC interconnect is \( 0.7RC \). Why?

\[ \tau = RC \]

\[ t_{PHL} = t_{PLH} = 0.7RC = 0.7\tau \]
Real Interconnect Circuit Model

How to compute the delay from node r to node l in this complex RC network?

Answer: Use Elmore delay formula!

Elmore Delay Formula

\[ \tau_{Di} = \sum_{i=1}^{N} C \cdot R_{ik} \]

\[ \tau_{Di} = R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_1)C_4 \]
**Example 1: Elmore Delay in RC Ladder**

\[
\tau_{Di} = \sum_{k=1}^{N} R_{ki} C_k \\
= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N
\]

**Example 2: Another Elmore Delay**

Try this example by yourself. The time constant from Vin to node 8 is 43ns. Therefore, the propagation delay from Vin to node 8 is 30.1 ns
Open Question:

- When an inverter is driving an interconnect, it is better to model the gate as a resistor.
- Based on what you have learned so far, how do you compute the effective output resistance of an inverter?
- Rout is one of the parameters in inverter cell characterization in Electronic Design Automation (EDA) tools.

Homework 15

- Assume that $V_{DD}=1.5\,V$, $K'_n=100\,\mu A/V^2$, $V_{Tn}=0.4\,V$, $\lambda_n=0.1\,V^{-1}$, $(W/L)_n=10$, $K'_p=60\,\mu A/V^2$, $V_{Tp}=-0.4\,V$, $\lambda_p=0.2\,V^{-1}$, $(W/L)_p=17$. Find $R_{out}$. Hint: connect a load of 100fF to the gate, calculate the LH propagation delay ($t_{PLH}$) using average current technique, then equate the propagation delay to a simple RC network and find $R_{out}$. This will effectively be $R_{out}(LH)$.
- Use Elmore technique to compute the time constant and LH propagation delay ($t_{PLH}$) of the above network from the gate input to node 5.