Review of Last Lecture

- Electrical Property of Materials
- Energy Band Diagrams
- Semiconductor Materials
- n-Type and p-Type Semiconductor Materials
- Mass Action Law
Today’s Lecture

- Carrier Transport in Semiconductors
- Drift Current
- Diffusion Current
- PN Junction
- Depletion Region
- Reverse Biased PN Junction
- Forward Biased PN Junction

Drift Current Due to Electric Field

- This is what happens in a typical resistors
- Direction of electrons and holes under externally applied electric field (E) is shown below
Drift Current Equations in Semiconductor

\[ J = \mu_n q \bar{E} n_o + \mu_p q \bar{E} p_o \]

n-type silicon has \( n_s = N_s = 10^{17} \) (atoms/cm\(^3\)) at 300 K, \( \mu_n = 1350 \) cm\(^2\)/V•s, \( \mu_p = 480 \) cm\(^2\)/V•s, and the electric field is 10 V/cm. (a) What is the minority hole carrier density \( p_h \) (b) What is the total current density \( J \)? (c) What is the resistivity of the material?

Solution

(a) \[ p_h = \frac{n_s^2}{n_i} = \frac{(1.062 \times 10^{19})^2}{10^{27}} = 1.128 \times 10^{16} \text{ (holes cm}^{-3}\text{)} \]

(b) \[ J = (1350)(1.6 \times 10^{-19})(10)(10^5) + (480)(1.6 \times 10^{-19})(10)(1.128 \times 10^7) \]
\[ = 216 + 8.7 \times 10^{13} \approx 216 \left( \frac{A}{\text{cm}^2} \right) \]

(c) \[ J = \sigma E \rho \]
\[ 216 = 10 / \rho \rightarrow \rho = 46.3 \text{ m} \Omega \text{ cm} \]

Ref: \( \rho_{se} = 1.7 \mu \Omega \text{ cm} \)

Diffusion Current Due to Density Gradient

- This happens when the carrier concentration is different from one side to the other side.
- An analogous case happens in gas container below, where the gas molecules “diffuses” from higher density to lower density.
**Diffusion Current Equations**

\[ J_{p,\text{diff}} = q D_p \frac{dp_0}{dx} \]
\[ J_{n,\text{diff}} = q D_n \frac{dn_0}{dx} \]

\( D_n \) and \( D_p \) are the electron and hole “diffusion constants”

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**PN Junction**

- What does happen when P-Type semiconductor meets N-Type Semiconductor?

![Diagrams of PN Junction](image.png)
**PN Junction**

- Some electrons will cross the junction and fill holes. A pair of ions is created each time this happens.
- As this ion charge builds up, it prevents further charge migration across the junction.
- The junction goes into equilibrium when the barrier potential prevents further diffusion.
- At 25 degrees C, the barrier potential for a silicon pn junction is about 0.5 to 0.7 volts.

![Depletion Layer](image)

**Depletion Region in Equilibrium**

- The barrier potential across deletion region is computed as:
  \[ V_{bi} = V_{th} \ln \left( \frac{N_A \cdot N_D}{n_i^2} \right) \]
  \[ V_{th} = \frac{kT}{q} \]

- The width of depletion region is computed as:
  \[ W = \sqrt{\frac{2\varepsilon_{vi} N_A + N_D}{q N_A \cdot N_D} V_{bi}} \]
Example: Depletion Region

- Calculate the built-in potential and depletion width at 300K in a diode if \( n_i = 1.062 \times 10^{10} \text{ cm}^{-3} \), \( \varepsilon_{si} = 1.04 \times 10^{-12} \text{ F/cm} \), \( N_A = 10^{16} \text{ cm}^{-3} \), and \( N_D = 10^{17} \text{ cm}^{-3} \).

\[
V_{bi} = V_a \ln \left( \frac{N_A \cdot N_D}{n_i^2} \right) = 0.026 \ln \left( \frac{10^{16} \cdot 10^{17}}{(1.062 \times 10^{10})^2} \right) = 0.775 \text{ V}
\]

\[
W = \sqrt{\frac{2 \varepsilon_{si} N_A + N_D}{q N_A N_D}} V_{bi} = \sqrt{\frac{2 \times 1.04 \times 10^{-12} \cdot 10^{16} + 10^{17}}{1.609 \times 10^{-19} \cdot 10^{16} \cdot 10^{17}}} \times 0.775 = 3.32 \times 10^{-3} \text{ cm} = 0.332 \text{ µm}
\]

Depletion Region Phenomena

- The depletion region is so named because it is formed by removal of all free charge carriers leaving none to carry a current.

- Depletion region is therefore an insulator region within a conductive material.

- Many modern semiconductor devices function based on “depletion region” phenomena.

- Example: Diodes, Solar cells, Bipolar Transistors, and MOS Transistors, Variable Capacitance Diodes
**PN Junction Under Applied Voltage**

- The applied external voltage, $V_D$, on the diode will directly affect the built-in potential.
  - In reverse bias, the external voltage adds up to the built-in potential increasing the effect of $V_{bi}$.
  - In forward bias, the external voltage is against the built-in potential reducing the effect of $V_{bi}$.

- Depletion region width also depends on the voltage applied to the diode.

- Review:
  
  $$
  W = \frac{2\varepsilon_s N_A + N_D (V_{bi} - V_D)}{q} 
  $$
  
  $$
  V_{bi} = \frac{kT}{q} 
  $$

**Reverse Biased PN Junction**

- In CMOS transistors, that are currently used in semiconductor industry, all PN junctions are normally in reverse bias condition.

- When $V_D < 0$ the width of depletion region increases which results in no conduction.
Forward Biased PN Junction

- When $0 < V_D < V_{bi}$, the width of depletion region decreases.
- Once $V_D = V_{bi}$, then depletion region disappears and the diode starts conducting.
- The current in a diode can then be approximated as:

$$I_D = I_S \left( e^{V_D/V_{th}} - 1 \right) \quad V_{th} = \frac{kT}{q}$$

Diode’s Parasitic Capacitance

- The depletion region, which act as an insulator, behaves like a capacitor in a PN junction.
- The “junction capacitance” can be calculated as:

$$C_j = \frac{\varepsilon_{si} A}{W} = \frac{\varepsilon_{si} A \sqrt{\frac{2 \varepsilon_{di}}{q N_A + N_D}}}{ \sqrt{N_A \cdot N_D (V_{hi} - V_D)}} = \frac{A \sqrt{q \varepsilon_{si} N_A \cdot N_D V_{hi}}}{2 \sqrt{N_A + N_D}} = \frac{C_{jo}}{\sqrt{1 - \frac{V_D}{V_{hi}}} \sqrt{1 - \frac{V_D}{V_{di}}}}$$

Where:

$$V_{hi} = V_{th} \ln \left( \frac{N_A \cdot N_D}{n_i^2} \right) \quad V_{di} = \frac{kT}{q}$$
**Variable Capacitance Diode (Varactor)**

- Generally, the junction capacitance in a diode is undesirable because it slows down the switching of the diode.
- Sometimes, we make a good use of this “parasitic capacitance”.
- The capacitance of a reverse bias diode can be adjusted by the amount of bias on a diode.
- If the AC input signal is small enough, the reverse bias diode can be seen as a capacitor, whose value can be adjusted by its reverse bias voltage.

![Variable Capacitance Diode Diagram](image)

**Small Signal Model for Diodes**

\[ I_D = I_S \left( e^{v_D/v_t} - 1 \right) \quad V_{th} = \frac{kT}{q} \]

*Dynamic (Small Signal) Conductance*

\[ g_d = \left( \frac{dI_D}{dV_D} \right)_{V_D=V_{th}} = \frac{I_S}{V_{th}} e^{v_D/v_t} \approx \frac{I_Q}{V_{th}} \]

*Dynamic (Small Signal) Resistance*

\[ r_d = \frac{1}{g_d} = \frac{V_{th}}{I_Q} \]