ECE321 – Electronics I

Lecture 8: MOSFET Threshold Voltage and Parasitic Capacitances

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Review of Last Lecture

- Device Model for Linear Region
- Device Model for Saturation Region
- Channel Length Modulation
Today's Lecture

- Threshold Voltage Equation
- "Dynamic Parameters of Long Channel MOSFET"
- MOSFET Parasitic Capacitances
  - Overlap capacitances
  - Channel capacitances
  - Junction capacitances

Threshold Voltage Equation

- MOSFET is a four terminal device; Gate, Source, Drain, and Bulk.
- The Bulk may not be always connected to the Source.
Threshold Voltage Equation

- We normally assume that the bulk of the MOSFET is connected to source. However, sometimes the bulk and source are in different potentials ($V_{SB} \neq 0$). $V_{SB}$ is called “body bias”.

- The applied $V_{SB}$ changes the threshold voltage as shown below:

$$V_T = V_{T0} + \gamma \left( \sqrt{2\varphi_F} + V_{SB} - \sqrt{2\varphi_F} \right)$$

- In this equation, $V_{T0}$ is the zero bias threshold voltage, $\gamma$ is the body bias coefficient, and $\varphi_F$ is:

$$\varphi_F = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$$

- Where $N_A$ is the doping concentration in the substrate.

Example: Threshold Voltage & Body Bias

- Assume that $V_{T0}=0.8$ V, $\gamma=0.6$ $V^{1/2}$, $\varphi_F=0.4$ V. Find $V_T$ if $V_{SB}=2.5$ V.

$$V_T = V_{T0} + \gamma \left( \sqrt{2\varphi_F} + V_{SB} - \sqrt{2\varphi_F} \right)$$

$$V_T = 0.8 + 0.6 \times \left( \sqrt{2 \times 0.4 + 2.5} - \sqrt{2 \times 0.4} \right) = 0.8 + 0.55 = 1.35$$

Observations:

1) Body bias is normally reverse bias. (why?)

2) More reverse body bias increases the threshold voltage.
**MOSFET Threshold Voltage**

- The gate potential at which the channel inverts is called the threshold voltage ($V_T$).
- $V_T$ is always referenced in relation to the gate to source potential $V_{GS}$ (this is because the surface potential needs to exceed the source to “lure” electrons away into the channel).
- $V_T$ is comprised of four main components:
  - Work function difference between the gate and substrate $\phi_f$ (substrate) – $\phi_f$ (gate)
  - $V_{GS}$ component required to change the surface potential of $2\phi_f$
  - $V_{GS}$ needed to offset the depletion region charge
  - $V_{GS}$ needed to offset charges trapped in the gate oxide

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**More Detail on MOSFET Threshold Voltage**

**Zero body bias threshold voltage:**

$$V_{T0} = \varphi_{\text{ins}} + 2\varphi_f + \sqrt{2}qN_A\varepsilon_{\text{ox}} \frac{2\varphi_f}{C_{\text{ox}}} - \frac{Q_{\text{ox}}}{C_{\text{ox}}}$$

Where:

$$\varphi_f = \frac{KT}{q} \ln \left( \frac{N_A}{n_i} \right)$$

and

$$C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}$$

**Threshold voltage with body bias:**

$$V_T = V_{T0} + \gamma \left( |2\varphi_f + V_{SB}| - \sqrt{2}\varphi_f \right)$$

Where:

$$\gamma = \frac{\sqrt{2}qN_A\varepsilon_{\text{ox}}}{C_{\text{ox}}}$$

**Important Facts:**

- Body bias increases threshold voltage
- Threshold voltage is **positive** for normal NMOS
- Threshold voltage is **negative** for normal PMOS
MOS Capacitance

- Delay of digital CMOS circuits depends on capacitance of MOS device
- There is a trade off between parasitic capacitance and drive strength of MOS device
  - Larger $C_{ox}$ increases the drive strength ($I_{DS}$ equation)
  - However, larger $C_{ox}$ increases the device parasitic capacitance
- MOS parasitic capacitance includes
  - Overlap capacitances
  - Channel capacitances
  - Junction capacitances
- Between almost every two terminals of MOS device, there is a source of parasitic capacitance

MOS Parasitic Capacitances
Overlap Capacitances

- Because of the lateral S/D diffusion, there is an overlap between gate and S/D junctions.
- This overlap capacitance is a constant linear capacitance.

\[ C_{GSOV} = C_{GDOV} = WC_{ox}X_d \]

Channel Capacitances

- Channel capacitance is a voltage dependent and non-linear capacitance.

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>( C_{GBCH} )</th>
<th>( C_{GSCH} )</th>
<th>( C_{GDCH} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( C_{ox}WL_{eff} )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Linear</td>
<td>0</td>
<td>( \frac{1}{2}C_{ox}WL_{eff} )</td>
<td>( \frac{1}{2}C_{ox}WL_{eff} )</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>( \frac{2}{3}C_{ox}WL_{eff} )</td>
<td>0</td>
</tr>
</tbody>
</table>
**Junction Capacitances**

- Junction capacitance is the *depletion region* capacitance of S/D.
- It is a *voltage dependent* capacitance (remember reverse biased diode).

\[
C_j = \frac{C_{j0}}{(1 - V_{ssb}/\phi_0)^m}
\]

\[
C_{j0} = A_d \left( \frac{\varepsilon_s q N_A N_D}{2 N_A + N_D} \right)^{\phi_0/kT} \quad \phi_0 = \frac{KT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right)
\]

**Junction Capacitance Components**

- The Junction capacitance of bottom plate is treated separately from the three non-gate edges.
- The gate edge is often ignored since it is part of the conducting channel.
- The bottom plate is usually step graded with m=0.5.
- The sidewall are step graded with m=0.33 and face the channel-stop implant which has much higher doping than substrate.
**Junction Capacitance Components**

\[ C_{\text{Diff}} = C_{\text{Bottom}} + C_{SW} \]

\[ C_{\text{Bottom}} = C_{sW}L_s \]

\[ C_{SW} = C_{JSW}(2L_s + W) \]

**MOS Parasitic Capacitances**

\[ C_{GS} = C_{GSCH} + C_{GSOV} \]

\[ C_{GD} = C_{GDCH} + C_{GDOV} \]

\[ C_{GB} = C_{GBCH} \]

\[ C_{SB} = C_{Sdiff} \]

\[ C_{DB} = C_{Ddiff} \]